DATASHEET

GY -L SERIES Low ESR SUPERCAPACITORS

Revision 1.2, May 2020

The GY -L series of supercapacitors are the low ESR variant of the GY series cylindrical cells offering excellent value. They are available as single cells, or dual cell modules with a choice of cell balancing options.

Features:

- High power output to support peak current loads
- On-board energy storage to handle power surges (high capacitance and energy density)
- Long cycle life

Applications:

- Energy Harvesting for wireless sensors
- Peak power support for GSM/GPRS transmission
- Last gasp power for remote meter status transmission
- Peak power support for locks & actuators
- Peak power support for portable drug delivery systems
- Short term bridging power for battery hot swap

Electrical Specifications

Single cells

Part numbering code

G	Y	N	vvv	dd	mmm	S	ccc	R	-L
Model	**Cylindrical**	**# of cells**	**Voltage**	**Diameter (mm)**	**Length (mm)**	**Tolerance**	**Capacitance (µF)**	**Lead format**	**Low ESR variant**
		1	2R7 = 2.7V	6C = 6.3 08 = 8.0 10 = 10 1B = 12.5 16 = 16 18 = 18	012 = 12 068 = 68 120 = 120	M ± 20% S +50% /-20% V +30% /-10%	Two digits + number of zeros. e.g. 155 = 1500000µF = 1.5F	R = radial T = 2 solder tabs W = central pin + 3 solder tabs	

Rated Voltage: 2.7V
Temperature Range: -40°C to +65°C
Parameters measured at 25°C

CAP-XX Part no.	Cap (F)	ESR Max @ 1KHz (mΩ)	ESR Max @ DC (mΩ)	Dia (mm)	Length (mm)	DCL max @ 120 Hrs (µA)	Mass (gm)
Radial Lead							
GY12R708012S105R-L	1	120	150	8	12	6	0.9
GY12R708020S335R-L	3.3	65	65	8	20	10	1.5
GY12R708025S505R-L	5	60	65	8	25	15	1.7
GY12R710020S505R-L	5	45	60	10	20	15	2.2
GY12R710025M106R-L	10	30	55	10	25	30	2.8
GY12R716025M256R-L	25	25	35	16	25	60	6.9
GY12R718040M506R-L	50	15	20	18	40	75	20.5
GY12R718060M107T-L	100	6	10	22	45	260	23.0

Dual Cell Modules

Part numbering code

G	Y	N	vvv	dd	mm	S	ccc	R	B	-L
Model	**Cylindrical**	**# of cells**	**Voltage**	**Diameter (mm)**	**Length (mm)**	**Tolerance**	**Cap. (µF)**	**Lead & package format**	**Balancing**	**Low ESR variant**
		2	5R5 = 5.5V	6C = 6.3 08 = 8.0 10 = 10 1B = 12.5	12 = 12 68 = 68	M ± 20% S +30% /-10% V +25% / -5%	Two digits + number of zeros.	R,S,T = shrink wrap/radial – see dwg P,Q,O = plastic/radial – see dwg	R = Resistor* A = Active*	

*R pair of balancing resistors, 0402 resistors, 100KΩ unless otherwise stated in the order,
*A = CAP-XX active balancing circuit which draws < 1µA. For active balancing, lead alignment, R, must be “S” or “Q”.

Rated Voltage: 5.5V
Temperature Range: -40°C to +65°C
Parameters measured at 25°C

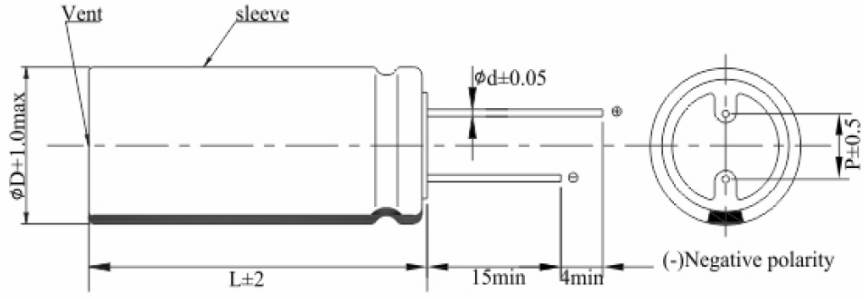
CAP-XX Part no.[1]	Cap (F)	ESR Max @ 1KHz (mΩ)	ESR Max @ DC (mΩ)	Thickness X Width (mm)	Length (mm)	DCL max @ 120Hrs (µA)[2]	Mass (gm)
Shrink Wrap							
GY25R50814S474RR-L	0.47	240	300	8 x 16	14	6	2.0
GY25R50822S155RR-L	1.5	130	130	8 x 16	22	10	3.1
GY25R51022S255RR-L	2.5	90	120	10 x 20	22	15	4.5
GY25R51026S505RR-L	5	60	110	10 x 20	27	30	6.0
Plastic Package							
GY25R50916S474OR-L	0.47	240	300	9 x18	16	6	5.6
GY25R50924S155OR-L	1.5	130	140	9 x18	24	10	6.1
GY25R51126S255OR-L	2.5	90	130	11 x 23	25	15	9.2

Note:
1. Part numbers shown for lead orientation R, P and for balancing resistors, R.
2. Leakage current at rated voltage, without accounted for the current drawn by balancing circuit.

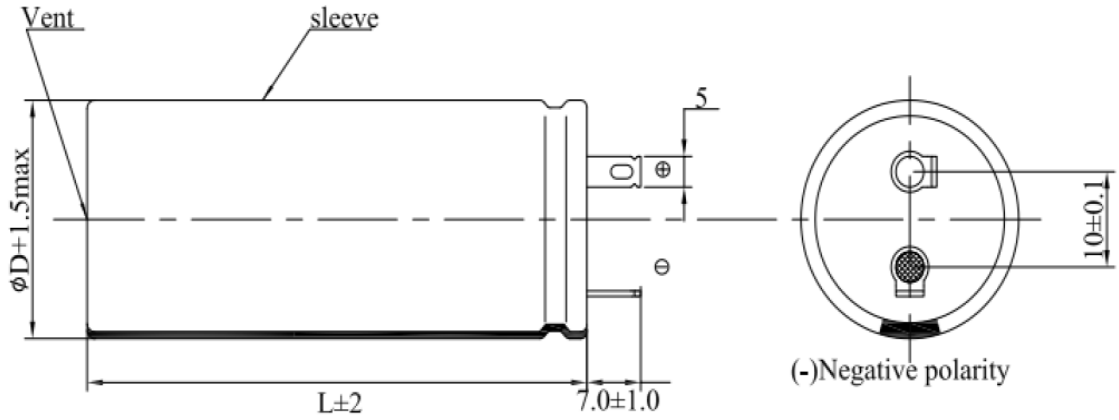
Dimensions (mm)

GY1 –L Series Shrink Wrap Radial Lead, 1F – 50F

ΦD	P	Φd
8	3.5	0.6
10	5.5	0.6
12.5	5.5	0.6
16	8	0.8
18	8	0.8



GY1 –L Series, T type, 2 Solder Tabs (100F, 22mm dia supercapacitor)

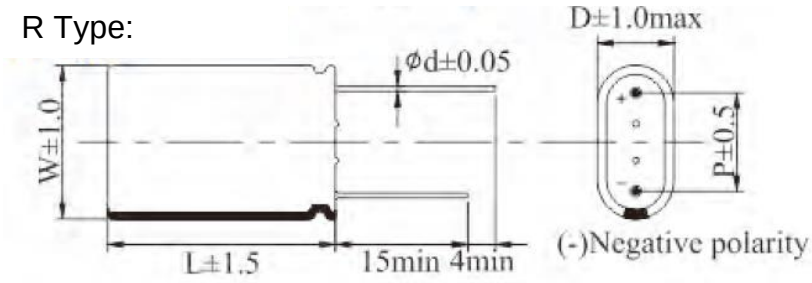


GY2 -L Series Shrink Wrap, 0.47F – 12.5F; L = R, S or T

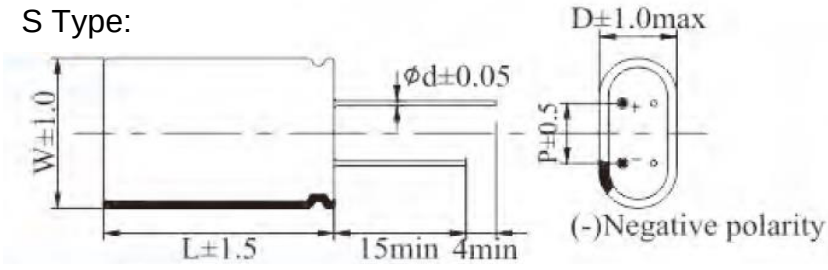
Note: All modules ordered with the active balance option must be S type.

Cell dia. (ΦD)	D	W	P			Φd
			R	S	T	
8	8	16	11.5	8.0	4.5	0.6
10	10	20	15.5	10.0	5.0	0.6
12.5	12.5	25	18.0	13.0	7.5	0.6

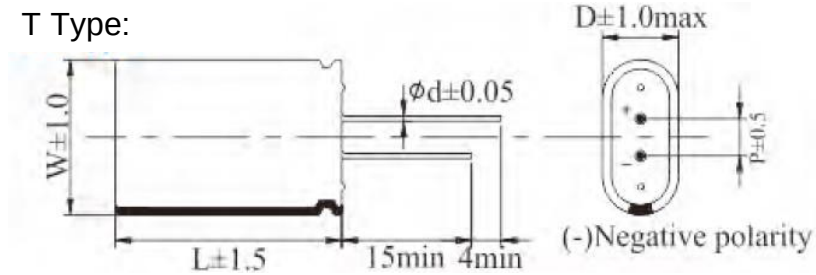
R Type:



S Type:



T Type:

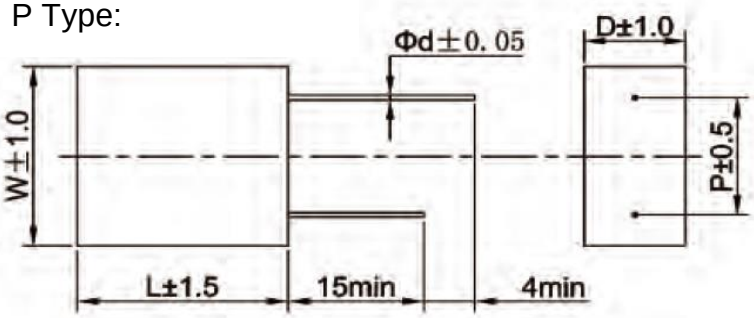


GY2 -L Series Plastic Package 0.47F – 12.5F; L = P, Q or O

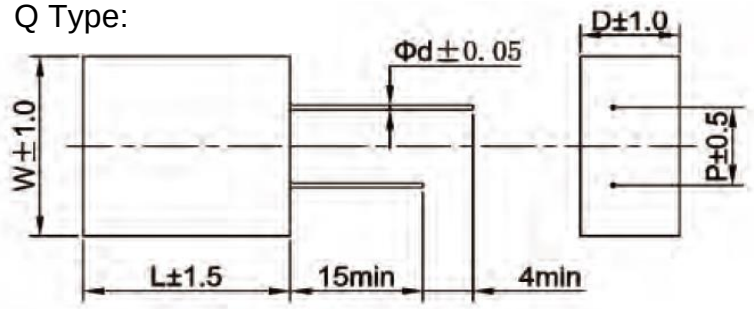
Note: All modules ordered with the active balance option must be Q type.

Cell dia.	D	W	P			Φd
			P	Q	O	
8	9	18	11.5	8.0	4.5	0.6
10	11	23	15.5	10.0	5.0	0.6

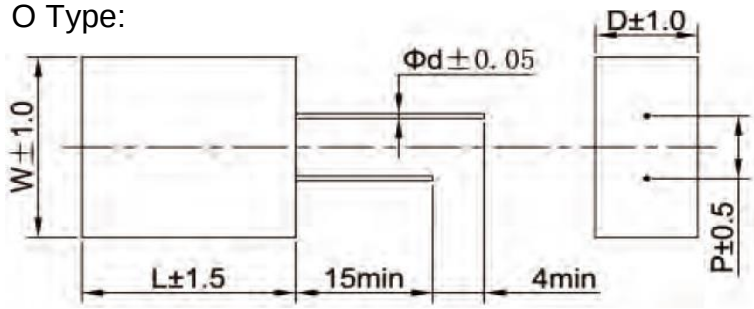
P Type:



Q Type:



O Type:



Measurement of capacitance

Capacitance is measured at 25°C using the method specified by IEC62391 shown in Fig 1. This measures DC capacitance. The capacitor is charged to rated voltage, V_R, at constant current, held at rated voltage for at least 30 minutes and then discharged at constant current. The time taken to discharge from 0.8 x VR to 0.4 x VR is measured to calculate capacitance as:

$$C = I \times (T_1 - T_2)/(V_1 - V_2)$$

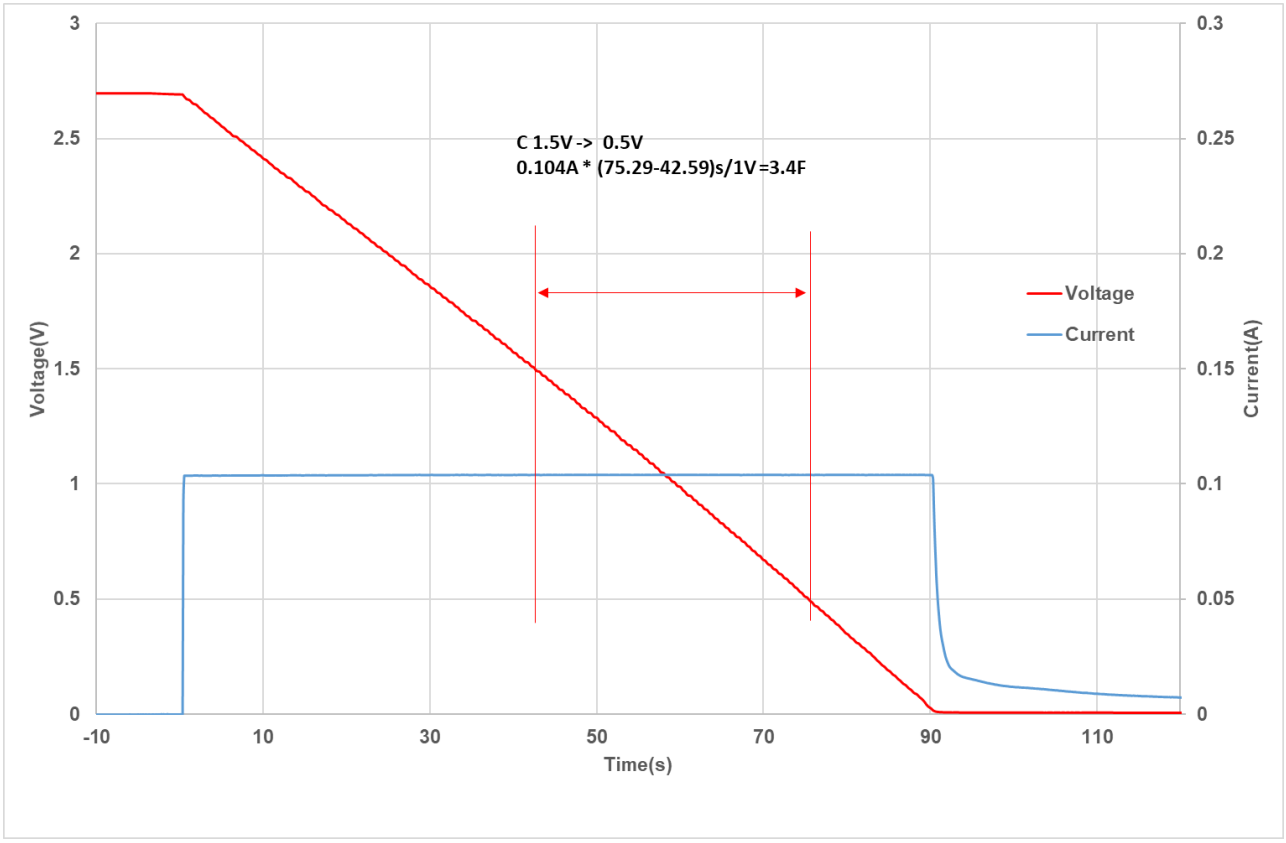


Fig 1: GY12R708020S335R-L Capacitance measurement

In this case, C = 0.104 A x 32.7s /1.V = 3.4F, which is well within the 3.3F +50%/-20% tolerance for a GY12R708020S335R-L cell.

Measurement of ESR

Equivalent Series Resistance (ESR) is measured at 25°C by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 200µs after the step current is applied to ensure the voltage and current have settled. In this case, for a GY12R708020S335R-L the ESR is measured as 140mV/2.97A = 47mΩ which is well below the 65mΩ max ESR specified for this cell.

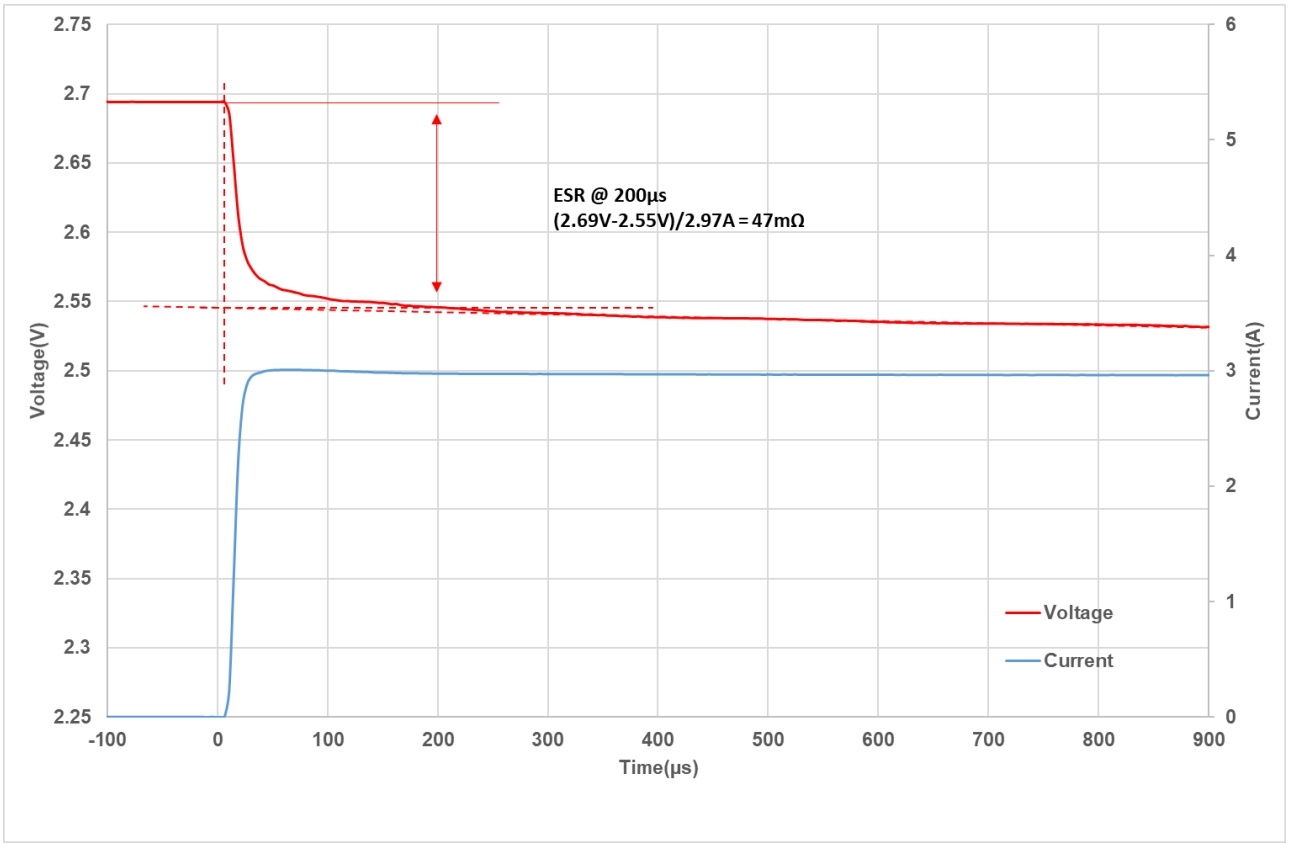


Fig 2: GY12R708020S335R-L ESR Measurement

Measurement of Leakage Current

Leakage current is measured by holding the supercapacitor at rated voltage at 25°C and measuring the current drawn through a high value resistor, typically 1KΩ or 2.2KΩ. The leakage current decays over time as shown in Fig 3 which shows the average leakage current for each supercapacitor. Leakage current is typically 1µA/F but the datasheet quotes the maximum values. Leakage current in the datasheet is quoted after 120hrs at rated voltage.

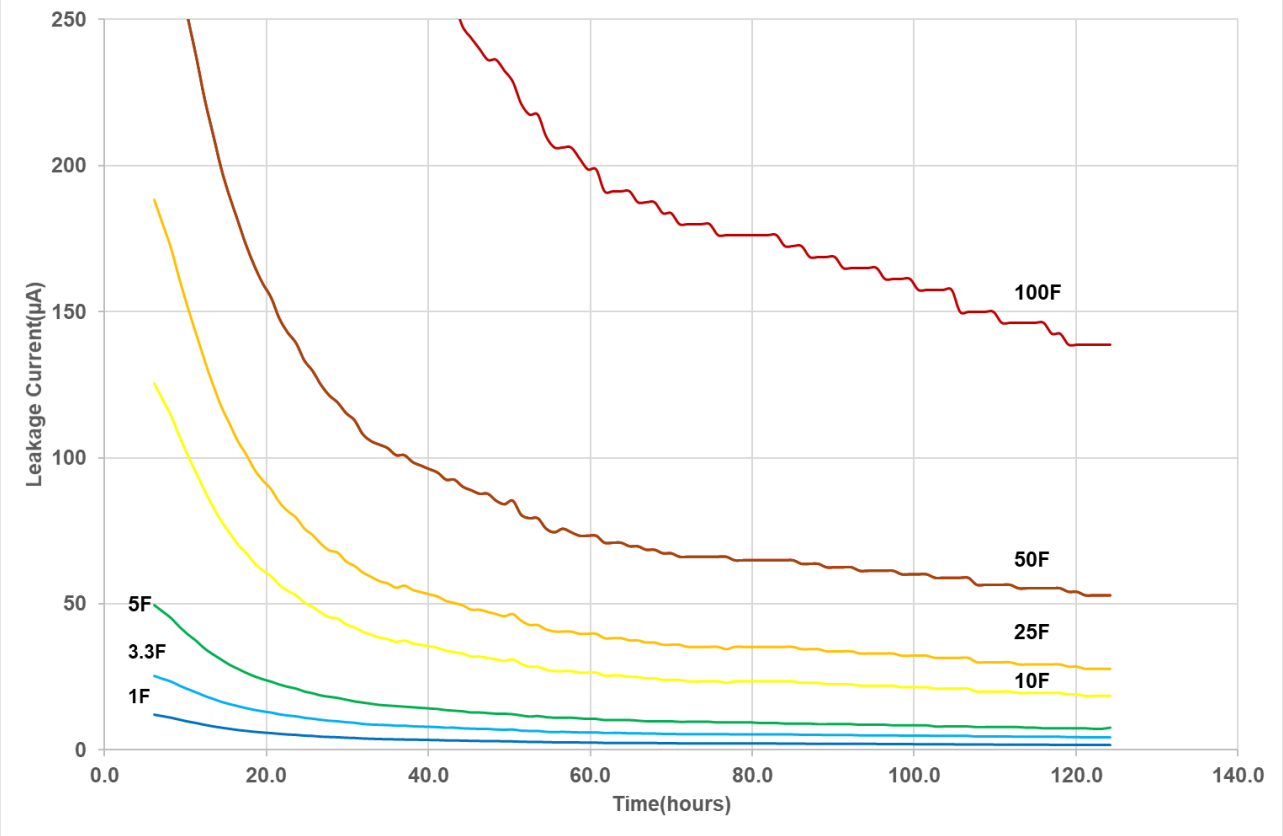


Fig 3: Leakage current measurement

Variation in DC Capacitance and ESR with temperature

Figure 4 shows that DC capacitance does not vary with significantly over the operating temperature range of -40°C to +65°C.

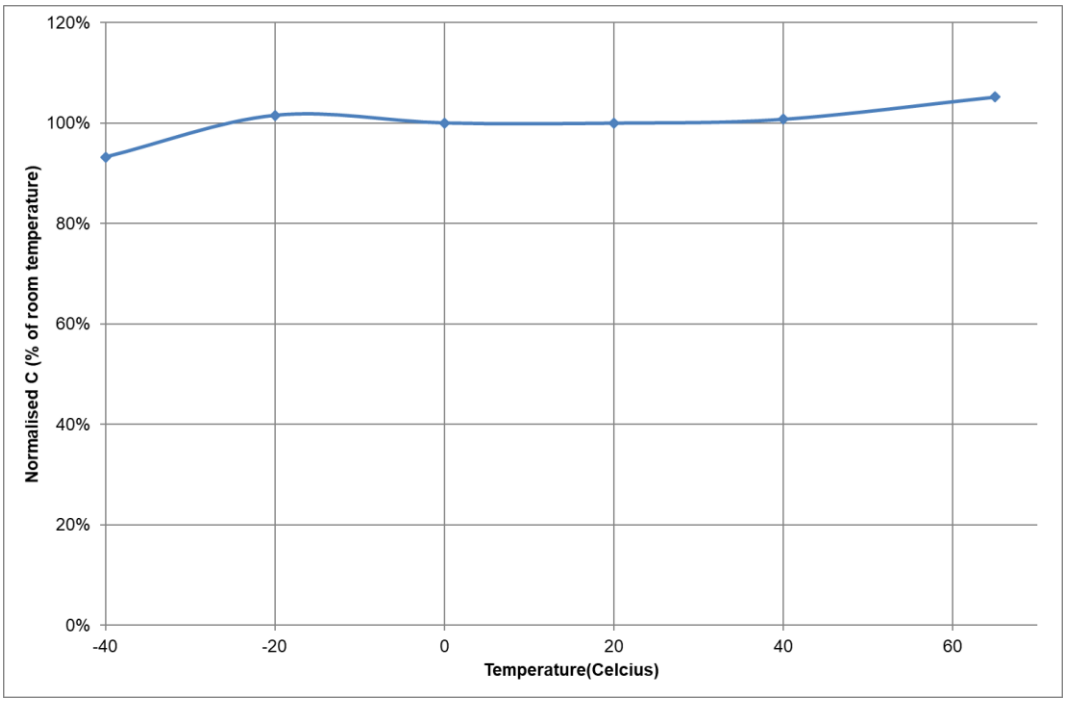


Fig 4: Variation in DC Capacitance over the operating temperature range

Figure 5 shows variation in DC ESR over the operating temperature range.

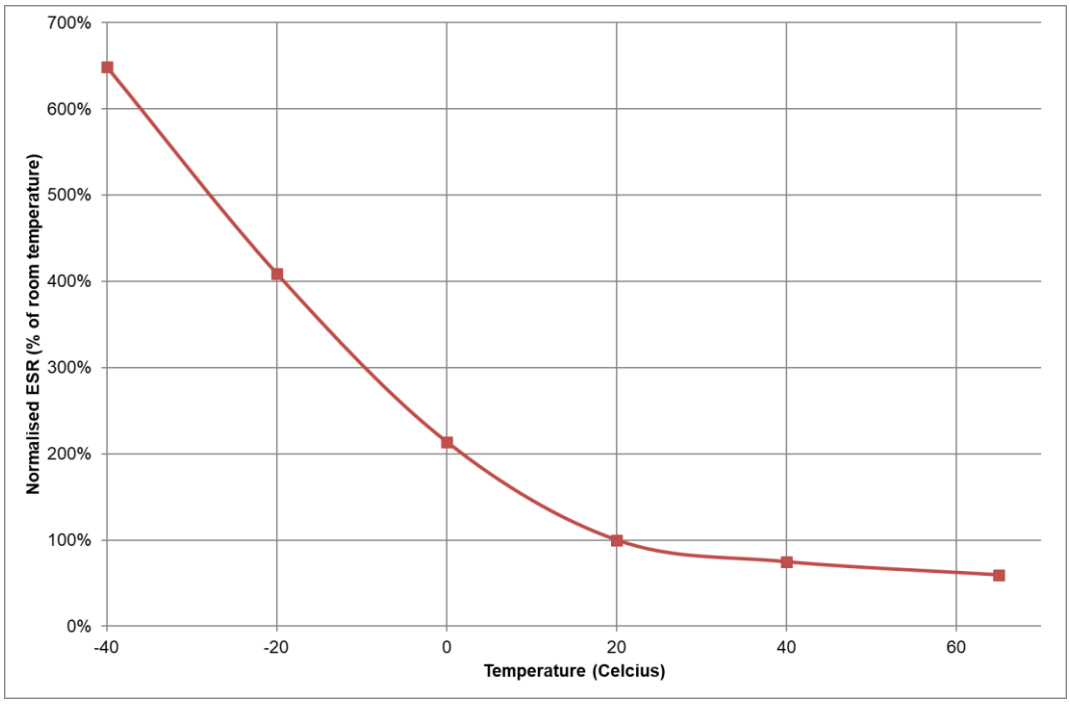


Fig 5: Variation in DC ESR over the operating temperature range

From Figure 5, ESR_{DC} at -40°C is 6.5x ESR_{DC} at room temperature. ESR_{DC} at 65°C is ~75% of ESR_{DC} at room temperature. The variation in ESR with temperature is due to the change in the mobility of ions in solution in the electrolyte.

Peak Current

Peak current is limited by Vrated/(ESR + R_L) where R_L is the load resistance including parasitic resistance such as PCB traces. The current then decays and is given by:

$$[Vrated/(ESR + R_L)].e^{-t/[(ESR+RL).C]}$$

where t = time in seconds. At high peak current, the supercapacitor discharges rapidly so that self-heating due to the high current is negligible. Table 1 Shows short circuit current for a range of supercapacitors initially charged to 2.7V at the instant the short circuit is applied and after 100ms. It also shows the temperature increase recorded due to the short circuit.

Table 1:

Capacitance (F)	Instantaneous peak current (A)	Current after 100ms (A)	Temperature rise (°C)
10	60	26	2
5	45	30	1.5
3.3	30	20	2
2	25	15	1.5
1	20	8	1

In all cases the temperature rise is not significant. A one-time peak current pulse is only limited by the ESR_{DC} + Load resistance, not by any thermal limitations.
The voltage drop when a constant current pulse of duration τ is applied =

$$V_{INIT} - V_{FINAL} = I.ESR_{DC} + I.\tau/C$$

Where:

I = constant current
τ = duration of constant current
V_{INIT} = the initial voltage when the current pulse is first applied
V_{FINAL} = the supercap voltage at the end of the pulse

Re-arranging terms, the maximum current that can be sustained for a time τ, when the supercapacitor is initially charged to rated voltage, V_R, and discharged to V_{MIN}, the minimum voltage that supports the given application =

$$I_{MAX} = \frac{V_R - V_{MIN}}{ESR_{DC} + \frac{\tau}{C}}$$

For constant power where I increases as V decreases to keep V x I = constant, there is no closed form solution. Use the Fixed Power worksheet in the file *CAP-XX Simulation Worksheet – BackupPower_VoltageDecay* simulator on the CAP-XX website to determine the min voltage after applying a constant power for a given time.

Maximum Continuous Current

Continuous current flow into/out of the supercapacitor will cause self-heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, and then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 6 shows the increase in temperature as a function of RMS current for various supercapacitors.

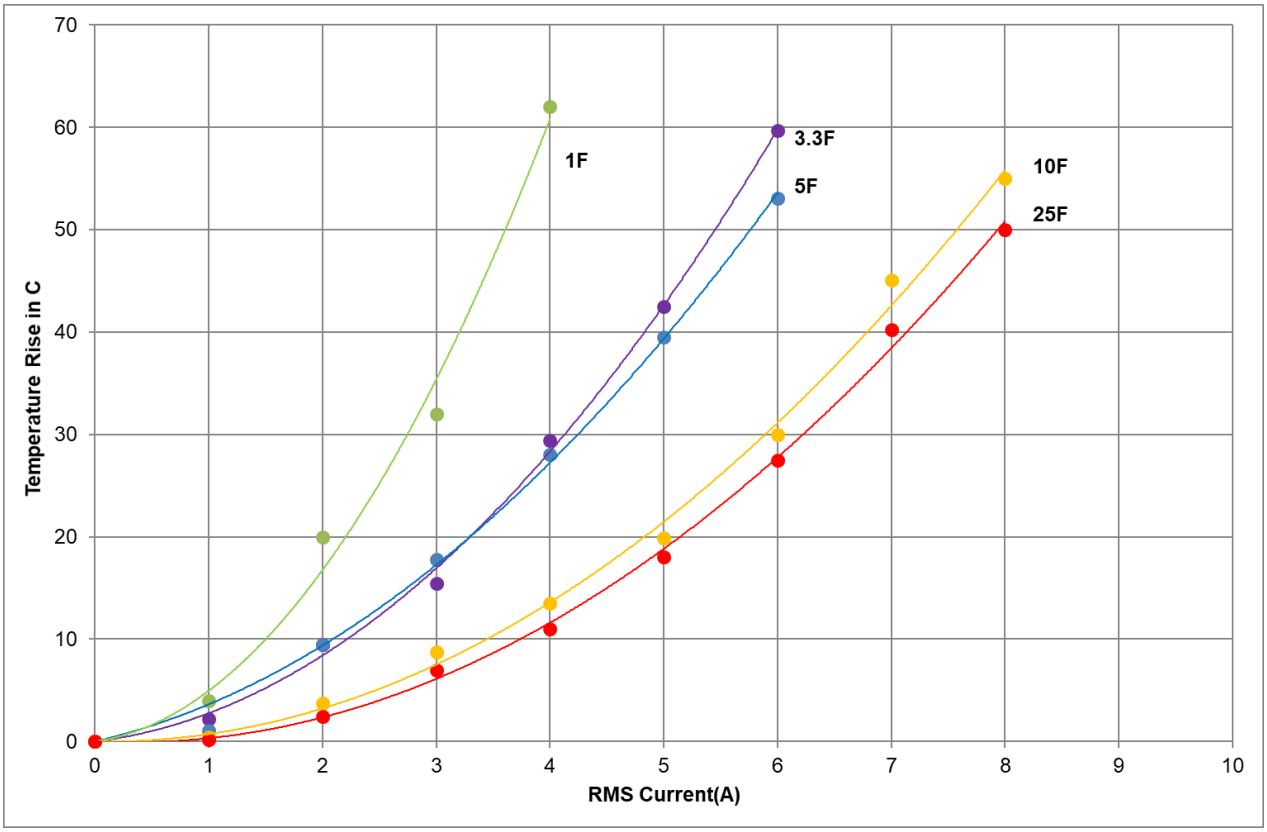


Fig 6: Self heating with RMS current for various supercapacitors

Supercapacitors with C > 25F will have a lesser temperature increase than the curve for the 25F supercapacitor in Fig 6. From Fig 6, the maximum RMS current in an application can be calculated. For example, if the ambient temperature is 40°C, and the maximum operating temperature for the supercapacitor is 65°C, then the maximum RMS current for a 10F supercapacitor should be limited to 5.3A, which causes a 25°C temperature increase.

Effective capacitance (Ceff)

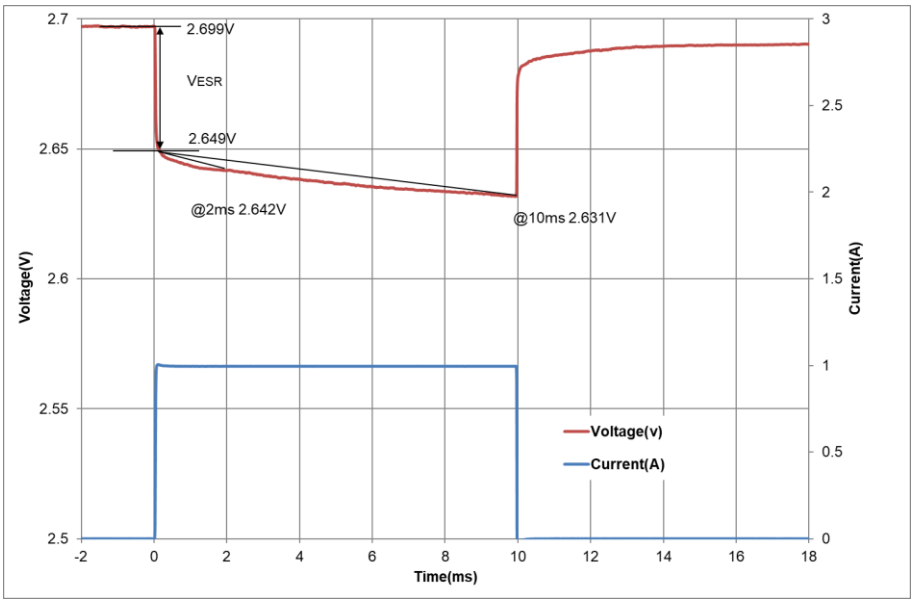


Fig 7: Discharge waveform illustrating the concept of Ceff

In Fig 7, consider the voltage drop due to capacitance after 2ms = 2.649V – 2.642V = 7mV. Therefore Ceff(2ms) = Discharge_Current x 2ms/Voltage drop(2ms) = 1A x 0.002s/0.007V = 286mF. The voltage drop due to capacitance after 10ms = 2.649V – 2.631V = 18mV. Ceff(10ms) = 1A x 0.01s/0.018V = 556mF. Fig 8 shows Ceff as a % of DC capacitance for the GY -L series of supercapacitors.

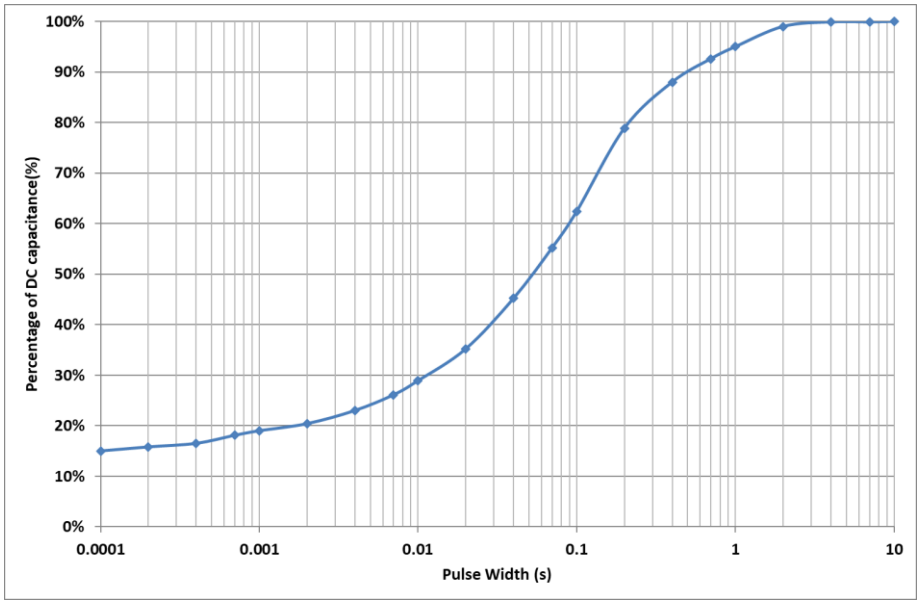


Fig 8: Normalised effective capacitance for GY-L series supercapacitors

For any given pulse width, T, with a constant discharge current I_{DISCH}, the voltage drop is given by:

Vdrop = I_{DISCH} x ESR + I_{DISCH} x T/Ceff(T)

Where Ceff(T) = DC capacitance x % at time T read from Fig 8.

Shorter pulses need less capacitance to support them, so the supercapacitors can support short pulses despite their frequency response.

Balancing options

In many applications a voltage > 2.7V but ≤ 5.5V is required. For these applications 2 supercapacitor cells are connected in series in dual cell modules such as the CAP-XX GY2 -L series which is rated to 5.5V. These cells should have a balancing circuit to ensure that the cell voltages remain approximately equal or the cell with the lower C will have a higher voltage across it, causing it to age faster than its companion cell, hence losing even more C until it goes over voltage. This is a reason why a balancing circuit should aim to maintain the voltage across each cell equal, rather than just prevent over-voltage. As an example, if the dual cell module was at 5.0V and there was over-voltage protection circuits that prevented each cell from exceeding 2.7V, then module could have one cell at 2.7V and the other at 2.3V. The cell at 2.7V will age faster than the cell at 2.3V and will age faster than if both cells were held at 2.5V shortening module life.

In the GY2 -L series modules there is a PCB connecting the 2 cells. This PCB can have one of two balancing options:

1. Option “R” as the last character in the GY2 -L series part number.
   A pair of balancing resistors are fitted, one resistor across each cell. The balancing resistors increase leakage current drawn by the module. Unless otherwise specified, 680KΩ resistors are fitted, increasing leakage current by 4µA at 5.5V.

2. Option “A” as the last character in the GY2 -L series part number.
   An op amp maintains the midpoint voltage = ½ the supercapacitor module terminal voltage. This solution maintains the midpoint voltage very accurately, responds more quickly as the supercapacitor charges and discharges and only adds ~1µA to leakage current.

If the application uses a supercapacitor charging IC that has an integrated supercapacitor midpoint balancing circuit, or there is a balancing circuit on the PCB, then order 2 x GY1 -L cells and place them in series. This makes the midpoint available to your balancing circuit. The dimensions of 2 GY1 -L cells placed next to each other are the same as a shrink wrapped GY2 -L series cell, refer to section 13, Dimensions.

Storage

CAP-XX recommends storing supercapacitors in their original packaging in an air conditioned room, preferably at < 30°C and < 50% relative humidity. CAP-XX supercapacitors can be stored at any temperature not exceeding their maximum operating temperature but storage at continuous high temperature and humidity is not recommended and will cause premature ageing.

Do not store supercapacitors in the following environments:

- High temperature / high humidity
- Direct sunlight
- In direct contact with water, salt, oil or other chemicals
- In direct contact with corrosive materials, acids, alkalis or toxic gases
- Dusty environment
- In environments subjected to shock and vibration

Soldering

When soldering it is important to not over-heat the supercapacitor to not adversely affect its performance. CAP-XX recommends that only the leads come in contact with solder and not the supercapacitor body.

Hand Soldering:

Heat transfers from the leads into to the supercapacitor body, so the soldering iron temperature should be < 350°C soldering time should be kept to the minimum possible and be less than 4 seconds.

Wave Soldering

The PCB should be pre-heated only from the bottom and for < 60 secs with temperature ≤ 100°C on the top side of the board for PCBs ≥ 0.8mm thick. The table below lists solder temperatures

Reflow Soldering

Infrared or conveyor over reflow techniques can be used on these capacitors. So not use a traditional reflow oven.

Transportation

All the supercapacitor cells in this datasheet store < 0.3Wh energy. The energy in watt-hours is calculated as: ½ x Capacitance x V_{rated}^2/3600. The largest cell in this range is 100F, so stored energy = ½ x 100 x 2.7^2 /3600 = 0.101Wh. Under regulation UN3499 there is no restriction on shipping these supercapacitors. Their shipping description is “Electrical Capacitors” with harmonized shipping code 8532.29.0040.