APPLICATON WHITE PAPER

AN1001

Inrush Current-Limiters for Supercapacitors

This application white paper describes: a high-performance current limit circuit; a low-cost current limit design; a simple in-rush current limit circuit; and an integrated solution based on available current limit ICs to be used for a Supercapacitor.

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Powering next generation products

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Outline

Supercapacitors with low ESR (Equivalent Series Resistance) and high capacitance are ideal components for use in pulsed-power applications, such as data transmission or actuators in which the load draws large current pulses. When connected across the supply, they provide much of the energy needed by each load pulse, reducing voltage ripple and instantaneous supply current. However, supercapacitors draw a high charging current when first connected. This can cause damage to a battery, or cause the supply voltage in a host device to drop from current overload. This application white paper describes: a high-performance current limit circuit; a low-cost current limit design; a simple in-rush current limit circuit; and a simple integrated solution based on available current limit ICs.

The CAP-XX high-performance solution

This solution limits the current to a safe, known value at all times, so it protects against supercapacitor inrush current, high load currents, and also against a short circuit in the load. This circuit has a very fast response. It operates with a supply voltage between 2.3V and 5.5V and employs a voltage reference, a sense resistor, an op-amp and MOSFETs. This solution has a settling time of 10µsec and typical impedance of ~60mΩ comprising of a current sense resistor = 22mΩ + FET $R_{DS(ON)}$ of 30mΩ.

Circuit Operation

The CAP-XX solution shown in figure 1 measures and controls the current delivered by the supply using an operational amplifier, and a P type MOSFET.

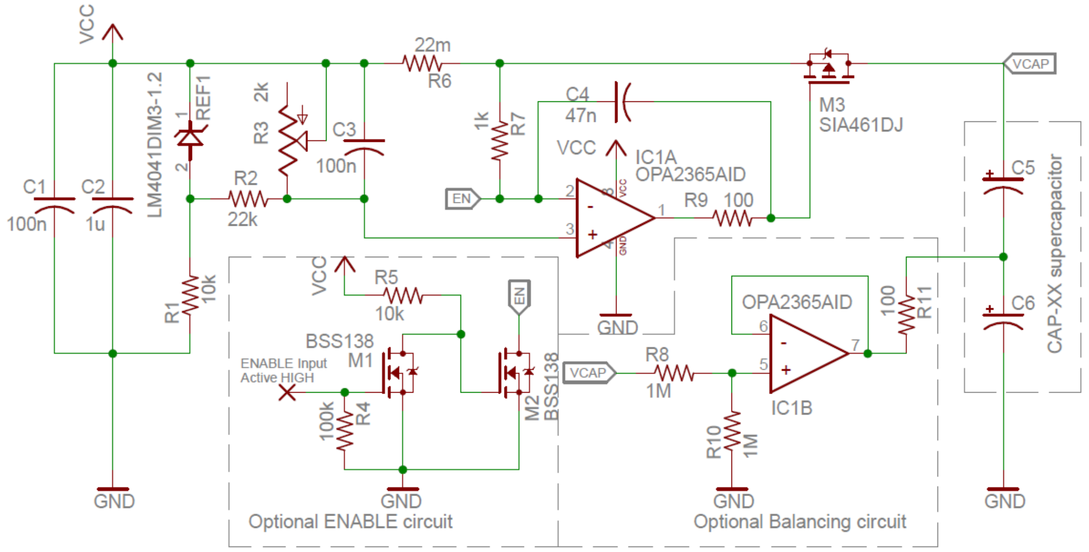

Figure 1: Current-Limiter using an Operational Amplifier and a MOSFET in Constant-Current Feedback Design with optional ENABLE and Active cell balancing circuits

This circuit is ideal for many applications, not only to limit inrush current, but also when the designer wishes to ensure that the design complies with a maximum current specification. The designer must ensure that with the current-limit supplies adequate current for the load, i.e. the current limit must be set ≥ average load current seen by the supercapacitor, e.g if the load is constant current then average current in x efficiency ≥ average current out, or if the load is constant power, then average power in x efficiency ≥ average power out. For further detail about this, the designer is referred to CAP-XX application white paper AN1003 Powering pulse loads and the calculation/simulation aids available on the CAP-XX web site: Supercap Pulse Simulator Fixed Current and Supercap Pulse Simulator Fixed Power.

The portion of Figure 1 enclosed in the dashed line rectangles are optional ENABLE and Active Cell balancing circuits. If these functions are not required, they may be omitted.

Note if dual cell device is used, a cell balancing circuit is required, please refer to CAP-XX application white paper AN1002 Cell Balancing.

Theory of operation

Figure 1 is a current-limit circuit that monitors the input current and uses feedback to control current flow through the current sensing resistor *R6*. The supercapacitor charged by the circuit is represented by *C5* and *C6*. It is a dual cell device and its associated balancing circuit is controlled by the other Op Amp circuit in that same IC package. The current limit value is independent of the supercapacitor value and only depends on the maximum current the source can supply.

The circuit in Fig 1 monitors the current by comparing the voltage drop across sense resistor (*R6*) with a reference voltage derived from a voltage reference IC (*REF1*). If the voltage across the sense resistor exceeds the reference value, the current is too high and the Op Amp's output begins to turn off the MOSFET, *M3*. When the supercapacitor is charged, the current drops below the set point and *M3* is turned on fully.

If the optional "ENABLE" circuit is included, then a logic HIGH signal (>1V) to the input is required to enable the current-limit circuit to operate. If the input is LOW or left floating, then *M2* is held ON by resistor *R5* which drags the inverting input of the Op Amp to GND, causing the Op Amp output to saturate to the positive rail turning off *M3*.

The voltage reference circuits *REF1* was selected for its accuracy and low power consumption. It is possible to replace it with lower cost Zener diodes or other type of shunt reference provided the part used has good tolerance (preferably 1%) across the temperature range of operation, otherwise the current limit may vary significantly. Zener diodes will typically require higher bias currents, resulting in increased power consumption by the circuit.

The operational amplifier used, OPA2365AIDG4 has a maximum input offset voltage of 100μV and a typical value of 20μV. Since this parameter affects the accuracy of the current limit, op amps with higher offset voltages should not be used if accurate current control is required. To a first order approximation, the current control accuracy =

$$\frac{Input\ Offset\ Voltage}{R6\ x\ I_{LIMIT}}$$

This operational amplifier also has a fast slew rate of 25V/μsec thus ensuring fast response for current control.

The optional Active cell balancing circuit is set up to be a simple unity gain buffer, with resistive divider *R8* and *R10* across the supercapacitor (*Vcap*) setting the midpoint voltage reference for the Op Amp to balance the cells to.

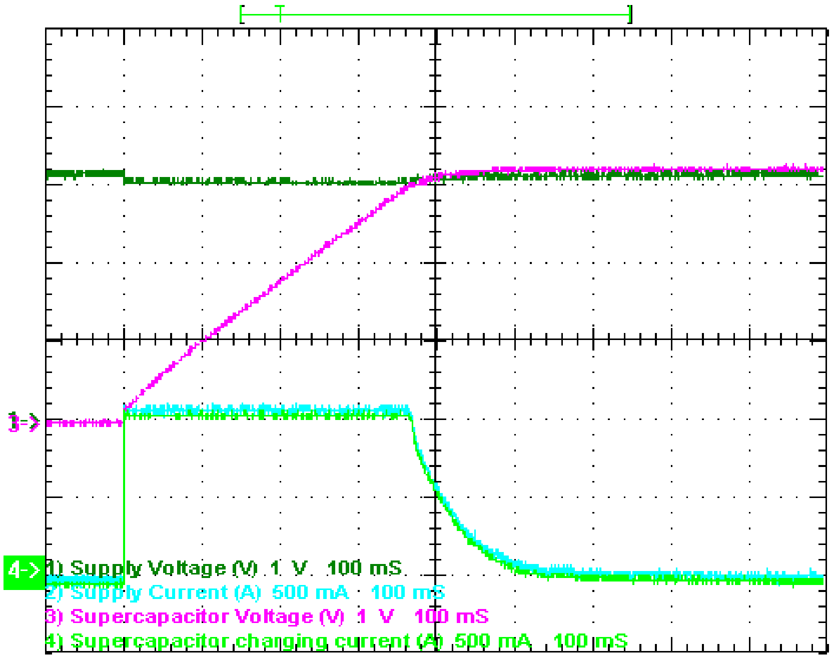

Figure 2: Charging a CAP-XX supercapacitor (0.12F and 50mΩ) using 3.3V supply and a current limit of 1A (CAP-XX solution)

Relationship between maximum current and component values:

The current limit in Figure 1 is set by resistors *R2* and *R3*.

The Op Amp will try to equalise the voltages at its non-inverting and inverting inputs. Hence the voltage drop caused by current through *R6* and the voltage drop by shunt voltage reference *REF1* and its associated resistor divider *R2* and *R3*, will be equal in steady state. So:

$$I_{limit} * R6 = \frac{V_{REF1} * R3}{R2 + R3}$$

If *R2* is fixed as shown in Figure 1, then R3 value can be calculated as follows:

$$R3 = \frac{I_{limit} * R6 * R2}{V_{REF1} - I_{limit} * R6}$$

Example: Using the values given in Figure 1, where V_{REF1} = 1.225V, *R6* = 22mΩ, *R2* is 22kΩ, then if the desired maximum current = 1A, the equation above gives 402Ω for the value of *R3*.

Transient Behaviour while charging a supercapacitor

Figures 3 and 4 below show the transient behaviour of the CAP-XX solution charging a supercapacitor from 0V using 1A current limit from a 3.3V supply and a 1A current limit from a 5.5V supply.

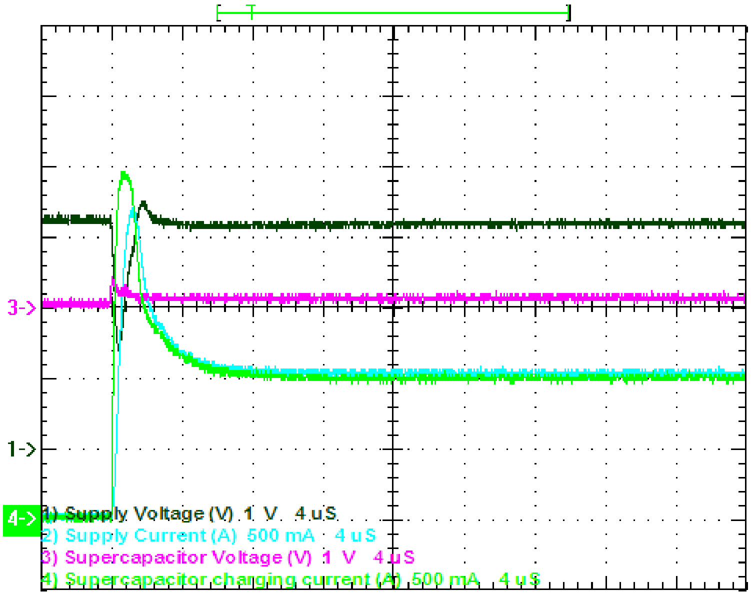

Figure 3: Charging a supercapacitor (0.12F and 50mΩ from 0V) using a 3.3V supply and the circuit set to 1A current limit (CAP-XX solution)

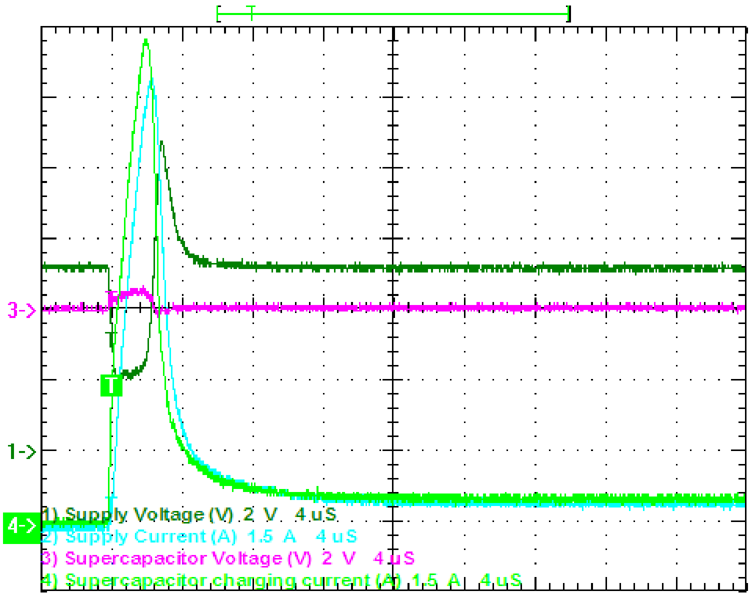

Figure 4: Charging a supercapacitor (0.12F and 50mΩ from 0V) using a 5.5V Supply and the circuit set to 500mA current limit (CAP-XX solution)

In the worst case, Fig 4, the current settled to its limit within 8µs. A host device (for example, USB) with sufficient decoupling on its supply (10µF - 100µF) could deliver the 10 Amps transient current for 8 µsec without resetting itself.

Performance with Class 10 GPRS load

The CAP-XX solution can also effectively limit the current while a class 10 GPRS load is applied to the supercapacitor. The GPRS pulse is a 1.15msec pulse with 25% duty-cycle at 1.8Amps. The following graphs show the response of the supply current and voltage with the GRPS load on the supercapacitor.

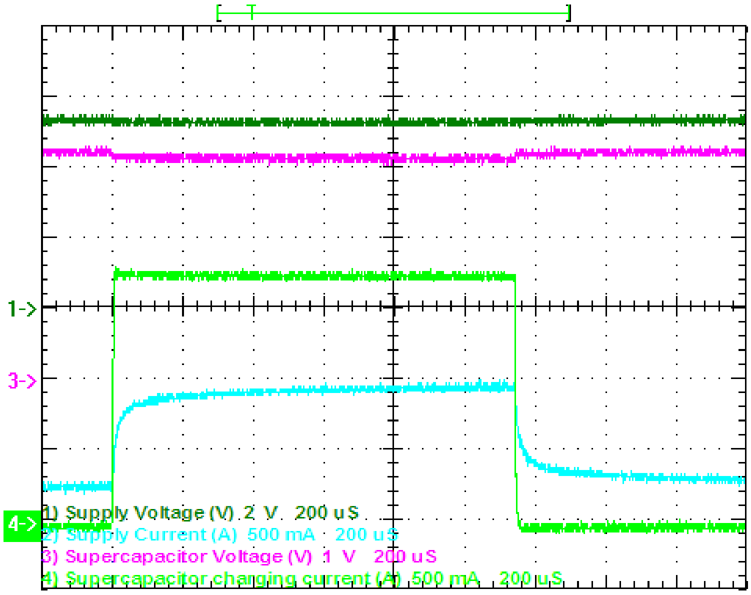

Figure 5: Load of a Class 10 GPRS pulse (1.8A) and a supercapacitor (0.12F and 50mΩ) with the supply at 3.3V and current limit set to 1A (CAP-XX solution)

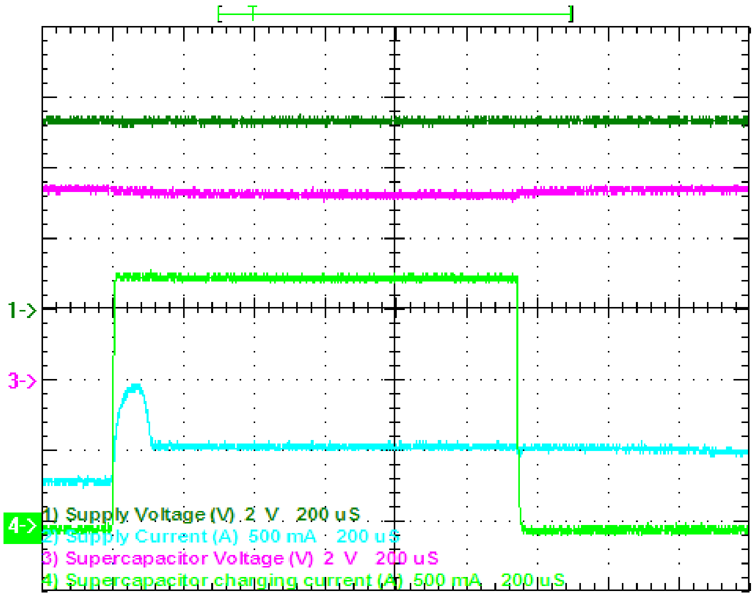

Figure 6: Load of a Class 10 GPRS pulse (1.8A) and a supercapacitor (0.12F and 50mΩ) with the supply at 5.5V and current limit set to 500mA (CAP-XX solution)

In the 5.5V applications with GPRS load, the 100µs supply current surge (peak of 950mA) can be taken care of by sufficient decoupling capacitors on the supply.

Thermal consideration

The CAP-XX solution has no thermal protection and care must be taken when using higher current limits. In the circuit shown in Figure 1, *R3* (2k potentiometer) limits the maximum allowable current to 4.6Amps which is safe for the MOSFET. However, if current limit higher than 4.7 Amps is required, *R2* must be changed.

Maximum continuous drain current, I_d (for SIA461DJ) = -12 A.

From its datasheet's safe operating area plot in Figure 7 below, it can safely pass 400mA at 4V V_{DS} indefinitely which equates to 1.8W power dissipation. However, this is assumes a small 1"x1" 2oz copper PCB area as heatsink. Most CAP-XX supercapacitors are fully charged within 10s even at 400mA. If a larger PCB area is used for heatsinking then more power can be dissipated. The actual calculation may be quite complex - please refer to manufacturer's datasheet.

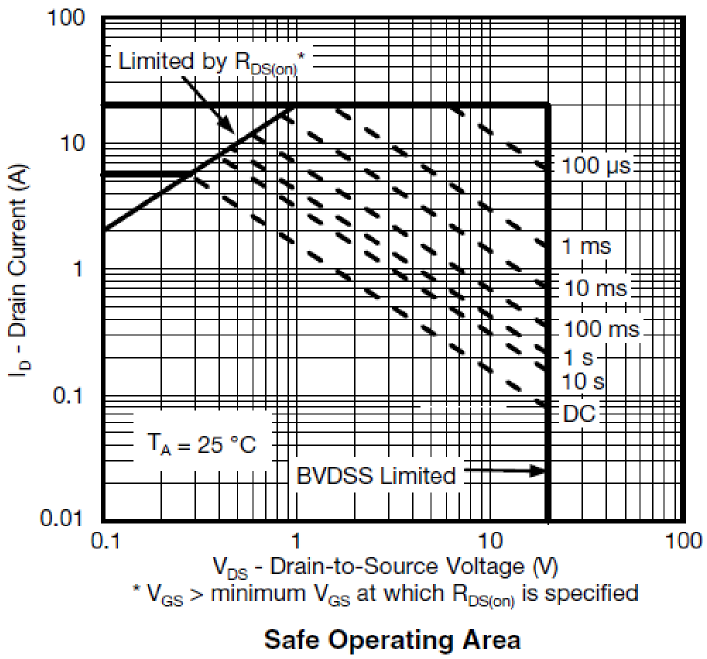

Figure 7: SIA461DJ datasheet's Safe Operating Area

Reverse Current Blocking:

In certain applications, when the supply is turned OFF, you do not want the supercapacitor to discharge by supplying current to the source through the P-channel MOSFET's body diode. To avoid this, another P type FET can be connected in series with the existing MOSFET (*M3*) with its gate connected to gate of *M2*, source pin to the source of *M3* and drain to sense resistor *R6*. As a result, when the ENABLE input is HIGH, both *M3* and the new FET are turned off with their body diodes back-back preventing current flow into the supply. Obviously the ENABLE function has to be included to allow reverse current blocking. Otherwise a Schottkey diode in series with M3 would suffice, in which case the forward voltage drop of the diode has to be considered.

The tables below give alternative MOSFETs and Op Amps.

Alternative MOSFETS

Part number	Power rating on 1”x1” 2oz copper PCB (refer to datasheet)	$V_{gs(th)}$	Absolute maximum I_d (A)
MCM1216	2.5W	-0.7V	-16 A
FDMA908PZ	2.4W	-0.6V	-12A
PMPB15XP	1.7W	-0.7V	-11.8A

Alternative lower cost rail to rail input Op-Amps:

Part number	Minimum operating voltage (V)	Maximum operating voltage (V)	Slew Rate (V/µs)	Input offset voltage (µV)
TLV9062IDR	1.8 V	5.5 V	6.5 V/µs	Typically 300µV
TLV2621	2.7V	5.5 V	10 V/µs	Typically 250µV

Note for this circuit to operate properly, the selected Op Amp must be rail-to-rail input and a HIGH level output > Vcc – $V_{gs(th)}$(of *M3*).

Advantages:

- Works from 2.3V to 5.5V.
- Fast settling time (10µs for charging a supercapacitor from 0V)
- Adjustable current limit.
- High current limit possible (max current depends on the MOSFET and its power rating).
- Low additional series impedance

Disadvantages:

- Numerous components therefore expensive.
- Large space requirement.
- No Thermal protection.
- Additional MOSFET required to provide reverse current blocking.
- May require heatsinking
- Linear current limit - wasteful of energy

Low cost and simple solutions

Simple current limit

When accurate current limiting is not required, just inrush current limiting and possibly load current limiting then two very simple low-cost current limit circuits can be built, with only 2 P type MOSFETs and a couple resistors. The first such design is shown below in Figure 8.

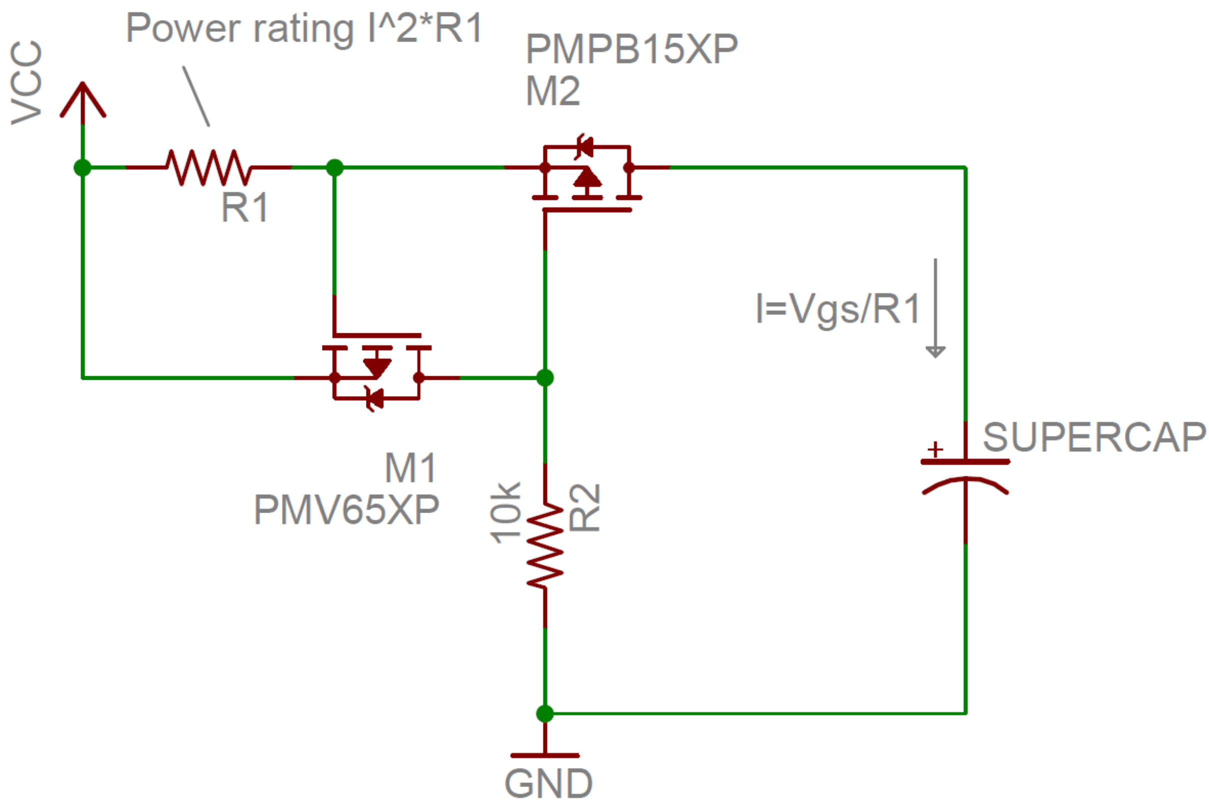

Figure 8: simple low-cost P-FETs current limit

Theory of operation

Initially, assuming the supercapacitor is at 0V, applying 5V to the Vcc will see *M2* turning on immediately by *R2* pulling gate of *M2* to GND. The current will start to flow through *R1* and create a voltage difference between the gate and source of *M1*. When the current increases to a level where V_{gs} of *M1* is approaching its turn on threshold, *M1* will start to let current through to its drain, causing the gate voltage on *M2* to rise. In turn this will reduce current flow through *M2* and eventually reach a steady state where input current is equal to the $V_{gs(th)}$ of *M1* divided by *R1*. Since transistors have very high gain, this simple circuit has a very fast frequency response. However, it's important to understand that $V_{gs(th)}$ of a MOSFET can vary widely based on its temperature as well as variation between FETs. Thus, the current control of this circuit may also vary by the same percentage variation as the quoted $V_{gs(th)}$ variation of *M1* by the manufacturer.

For the circuit above, with *R1* = 10Ω, the small SOT-23 MOSFETs chosen can only handle 0.5W hence the current limit must be less than 100mA for 5V continuous operation, which would be case if charging a large supercapacitor (e.g GS130, 2.4F) to 5V from 0V. The $V_{gs(th)}$ for M1 ranges between -0.47V to -0.9V (or a current range from 47mA – 90mA). This design foregoes precision for simplicity. In our test circuit, the current is controlled to ~70mA. This design's fast frequency response can be seen in figure 9 with settling time ~1µs after the supply voltage is applied. There is a small current ripple but no oscillation.

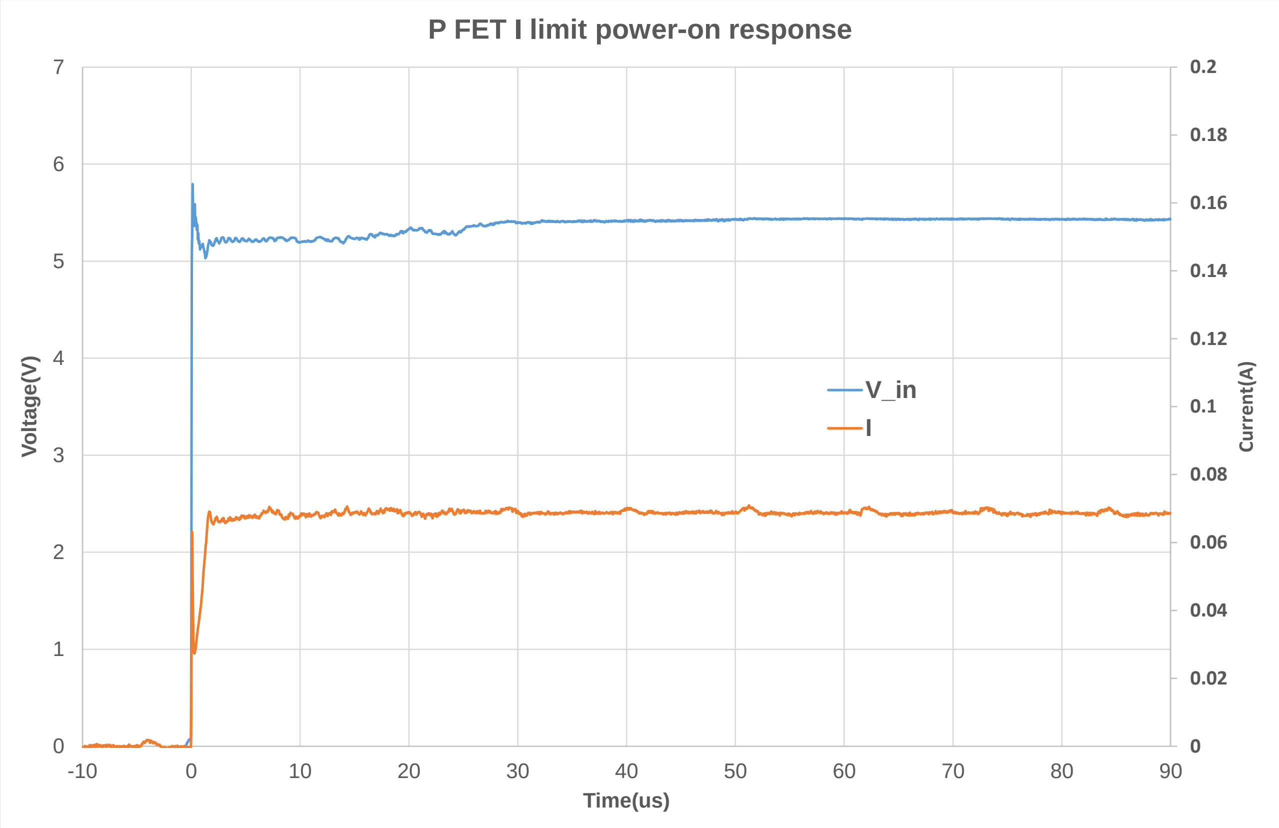

Figure 9: turn on response of the test circuit (70mA)

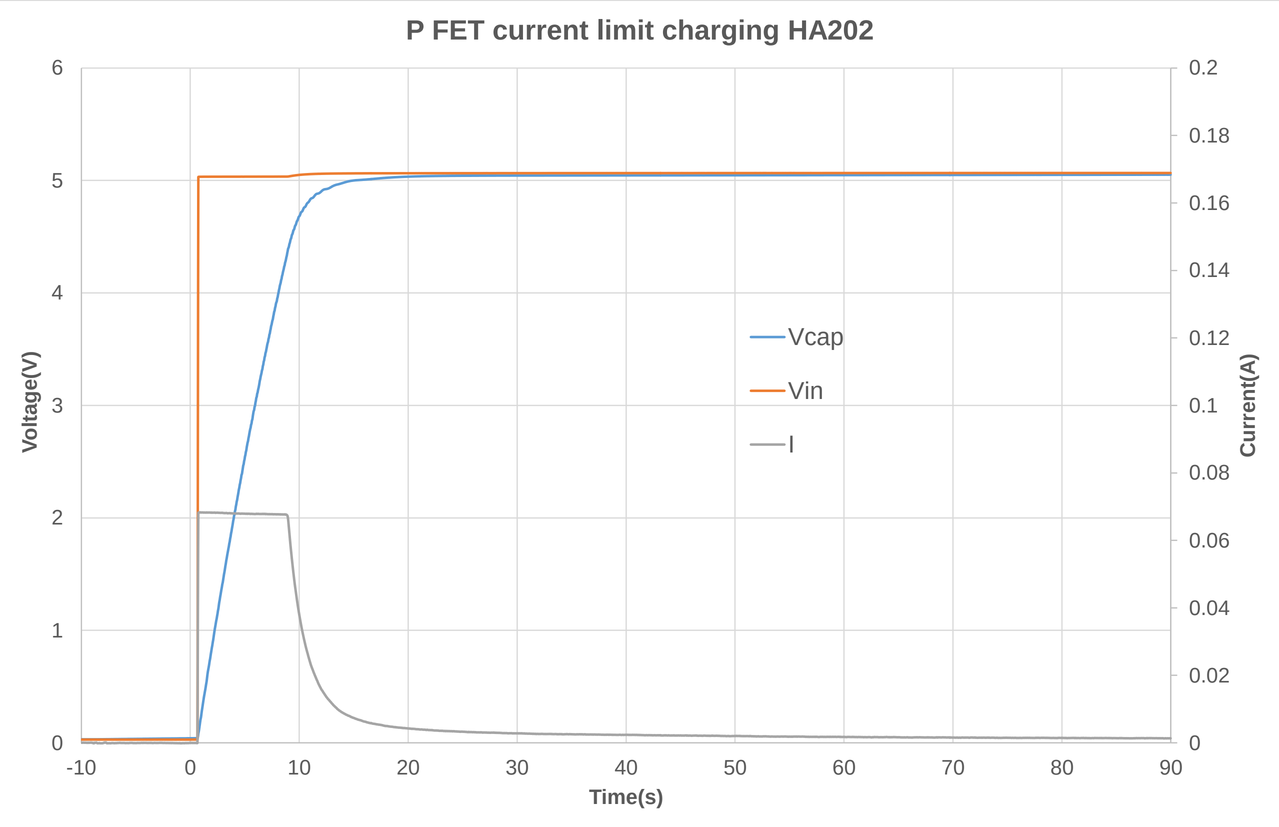

Figure 10: test circuit (70mA) charging a HA202 (120mF)

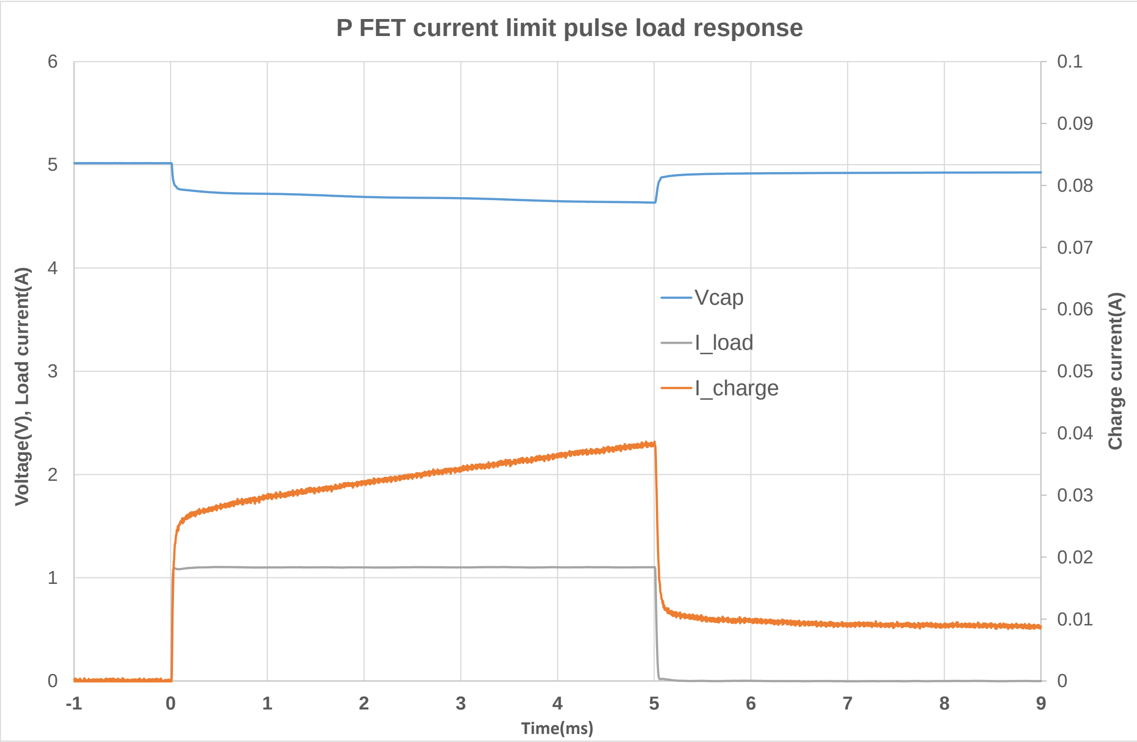

Figure 11: test circuit (70mA) response to 1A pulse load on HA202(120mF)

To reduce the power dissipation across *R1* and reduce the RC charging time constant when capacitor voltage approaches the supply voltage, the lower the $V_{gs(th)}$ of *M1* the better. Since *M1* does not need to handle any power, its power rating is not important for this design. The following table contains some recommended P MOSFETs. Choose any low $V_{gs(th)}$ (<1V typ), high power rating P type MOSFET for *M2*.

Recommended MOSFET for M2

Part number	**Power rating on 1"x1" 2oz copper PCB (refer to datasheet)**	**$V_{gs(th)}$ typical**	**Absolute maximum I_d (A)**
MCM1216	2.5W	-0.7V	-16 A
FDMA908PZ	2.4W	-0.6V	-12A
PMPB15XP	1.7W	-0.7V	-11.8A

Advantages:

- Simple, low-cost
- Small PCB real estate
- current limiting at all times, even if the load is short circuit the source is protected
- Wide operating voltage range 1V-20V

Disadvantages:

- Accurate current control not achievable
- Linear current limit - wasteful of energy
- High ON resistance = R1
- May require heatsinking
- No reverse current blocking
- No ENABLE control

Simple soft-start circuit

Another configuration with just two P FETs and two resistors is a simple soft-start circuit which only limits in rush current when supercapacitor voltage is initially low. This design does not control current at all times like the previous designs. It should be used when only a soft-start function is required during initial power on.

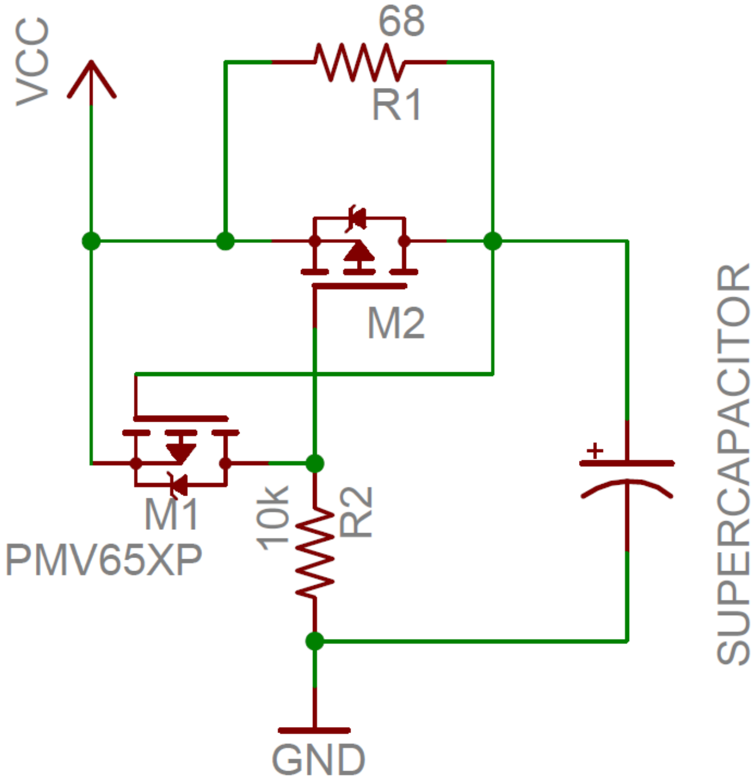

Figure 12: simple soft-start circuit to charge supercapacitor

Theory of operation

Assuming the supercapacitor is initially at 0V, when power (e.g. 5V) is applied to *VCC*, *M1* immediately sees -5V across its gate and source. However, the gate capacitance of *M2* has to be charged through *R2* before it can turn on. This ensures *M1* always turns on first, which holds the gate of *M2* at 5V maintaining *M2* OFF. *M2* stays off while the supercapacitor is charged via *R1.* Once the difference between the supply *VCC* and supercapacitor voltage is less than $V_{gs(th)}$ of *M1*, *M1* will turn off, enabling *R2* to pull the gate of *M2* to ground, turning on *M2* which bypasses R1 and connects the supercapacitor to *VCC* through R_{DSON} of *M2*.

R1 in this design dissipates all the power when limiting the in-rush current to the supercapacitor so it must be sized appropriately. The RC charge characteristic means the charge current and consequently the power dissipation drops exponentially. This reduction in charge current, added to the fact that most resistors can handle many times their rated power for short time, means you could one could use a lower power resistor for R1. Refer to the manufacturer's datasheet for detailed sizing and choice of *R1*.

Both *M1*, *M2* only work as switches, hence they can be any low $V_{gs(th)}$ (<1V, typ) P MOSFET with sufficient current capability.

A test circuit was built with *R1* = 68Ω(1/4W), and *M1* and *M2* were PMV65XP ($V_{gs(th)}$ = 0.65V, -4A). Figures 12 – 14 are the waveforms of the circuit's responses when charging an HA202 (120mF) to 5V.

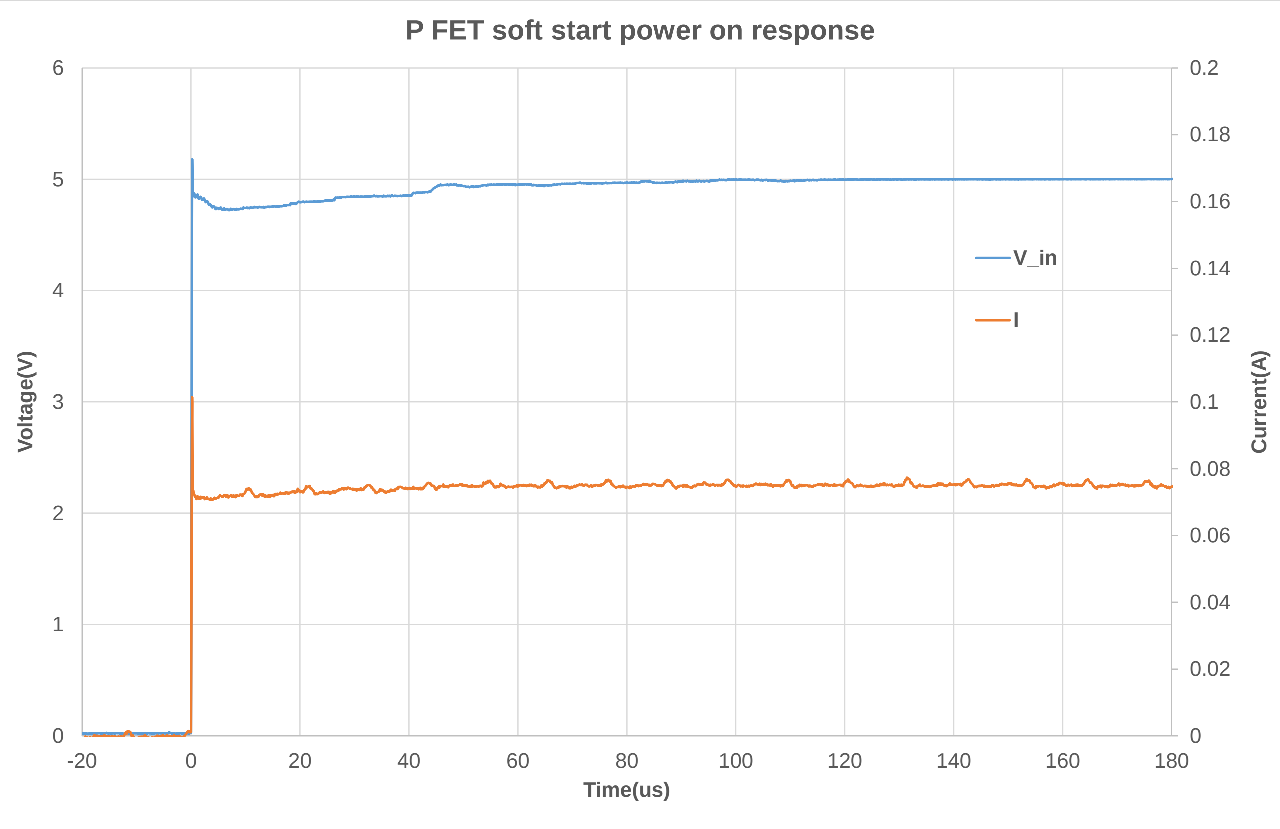

Figure 12: soft-start circuit power on response

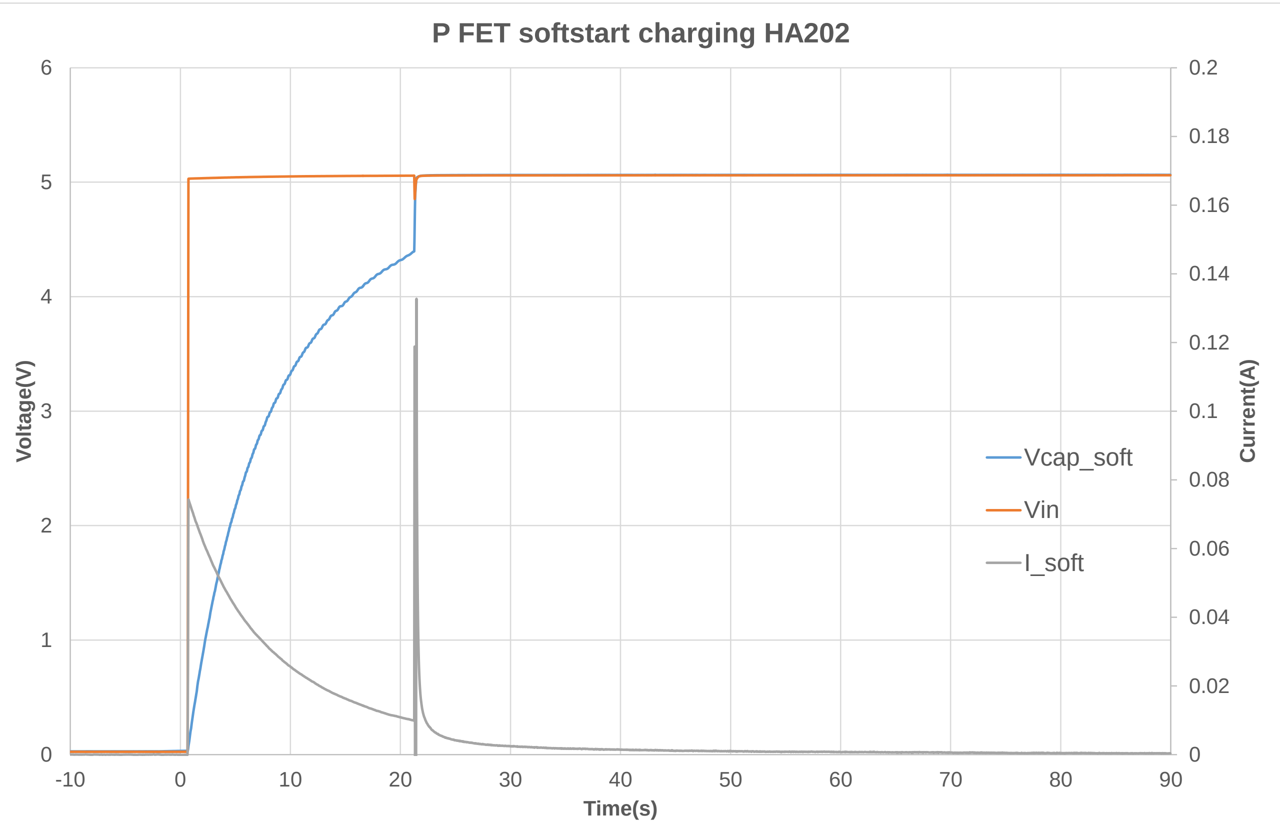

Figure 13: soft-start circuit charging a HA202 (120mF)

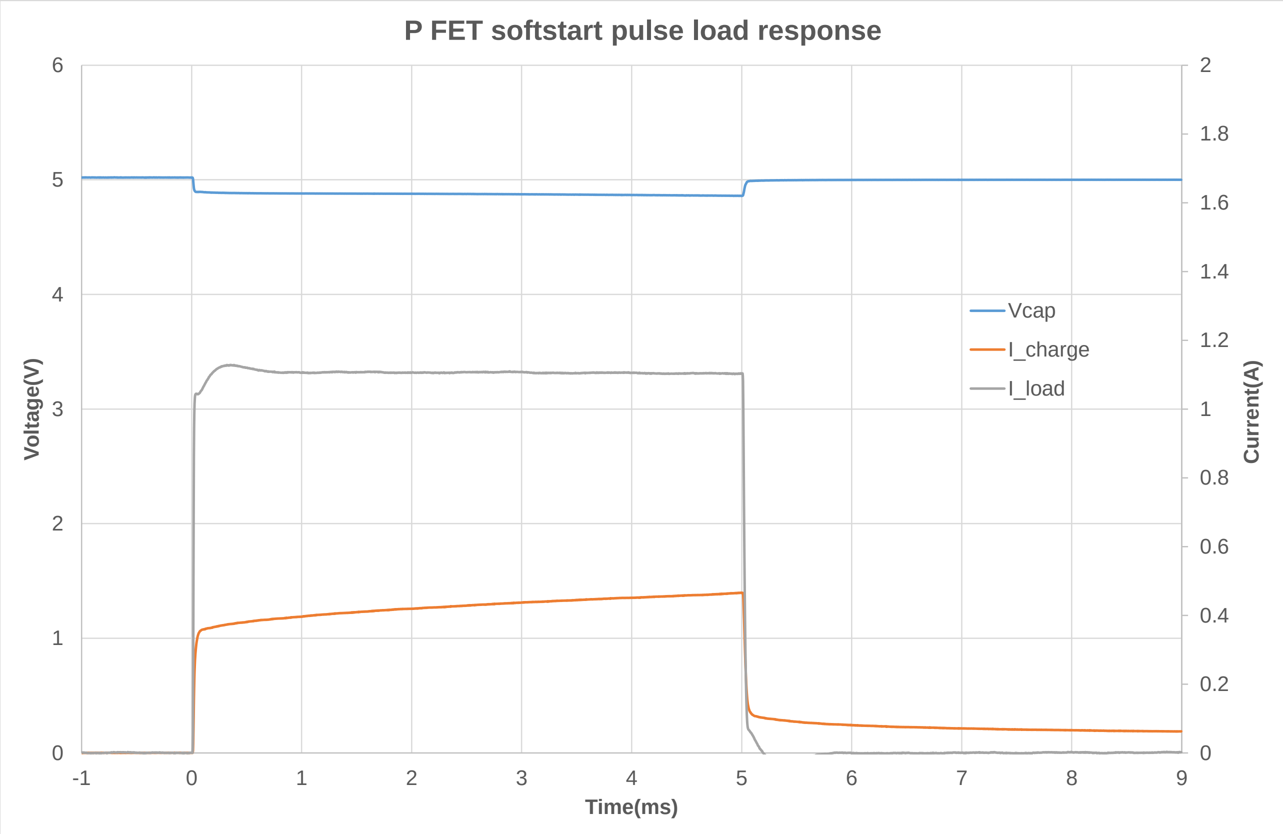

Figure 14: soft-start circuit response during a 1A pulse load on HA202(120mF)

Figure 13 and 14 show clearly that once *M2* turns on, the current flow is no longer limited by the circuit. Once *M2* is ON, the load current will be split between the supercapacitor and the power source in proportion to 1/their respective impedances. As a rule of thumb:

$$\frac{I_{supercap}}{I_{source}} = \frac{ESR_{source} + R_{ds(on)}(M2)}{ESR_{supercap}}$$

Ensure that *M2* is sized so the I_D max of *M2* < max load current in normal operation. If the load fails short circuit and draws current > I_D max of *M2,* and the source can supply this current, then *M2* could potentially fail. If the maximum current the source can supply < I_D max of M2 then this circuit is safe.

Advantages:

- Simple, low-cost
- Small PCB estate
- Limits in-rush current during start-up
- Low on resistance = R_{DSON} of *M2*
- Wide operating voltage 1V-20V

Disadvantages:

- No current limit once MOSFET turns on
- May require heatsinking
- No reverse current blocking
- No ENABLE control

Integrated Current Limit Solution

Many IC manufacturers offer devices called power distribution switches designed primarily for USB port power control and almost all of them have integrated current and thermal limiting to protect the energy source. They are small and simple to use, usually only require a few resistors and capacitors to complete the circuit. These devices often are priced lower than our OPAMP + MOSFET solution discussed earlier, but are significantly higher than our low-cost simple solutions.

To meet the requirement for USB port power control, most of these power distribution switches have an adjustable current limit up to 2A and operate from 2.5V – 5.5V which make them well suited to limit charge current to a supercapacitor. Many of them also come with reverse current blocking, reverse voltage protection and ESD protection.

These power distribution switches are usually manufactured as tiny IC packages. The small size limits the devices' power dissipation: 500mW for an SOT23-6 package is typical. Their integrated thermal protection disables the device when overheating occurs during an extended current limiting operation. Therefore, it's safe to design the current limit to momentarily exceed the rated power of the package. However, if the switch operates in current limit mode for extended period, for example charge a large capacitance supercapacitor or a large frequent load, the switch could spend significant time in thermal protection mode which would make charging the supercapacitor slower than simply designing for a lower current limit.

As an example, a test circuit with TPS2553D was built following the schematic in figure 15. Based on the datasheet's formula for current limit and the value of R1, this circuit should limit the current to around 470mA.

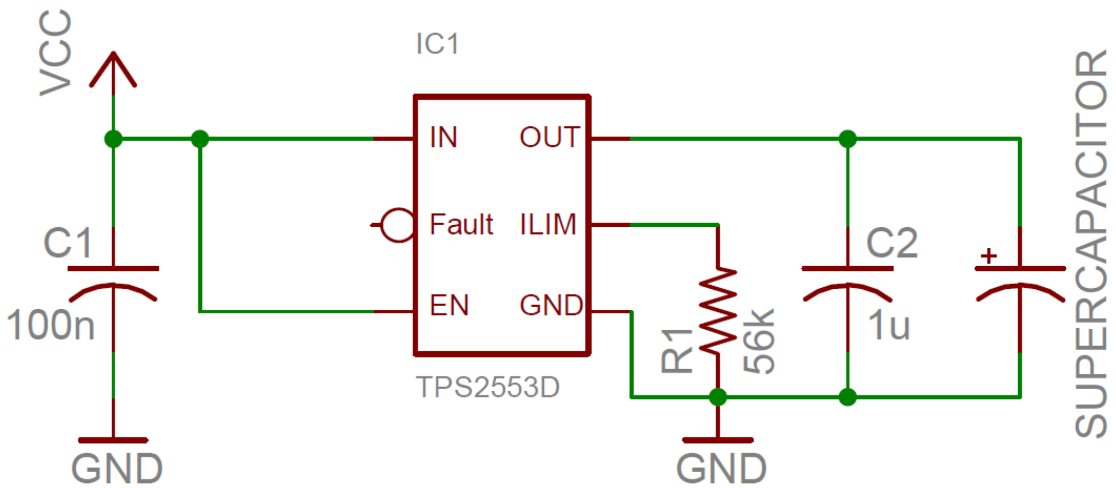

Figure 15: test circuit with TPS2553D

Figure 16 shows that while the current limiting is accurate, this circuit has a 1ms delay at power on. This delay only occurs during power-on. During the circuit's normal operation its response is much faster. Figure 17 shows the 1ms delay when charging a supercapacitor from 0V is insignificant and the current limit is constant during charging. Figure 18 shows the circuit's ability to handle a pulsed load very well, with minimal delay and accurate current limiting.

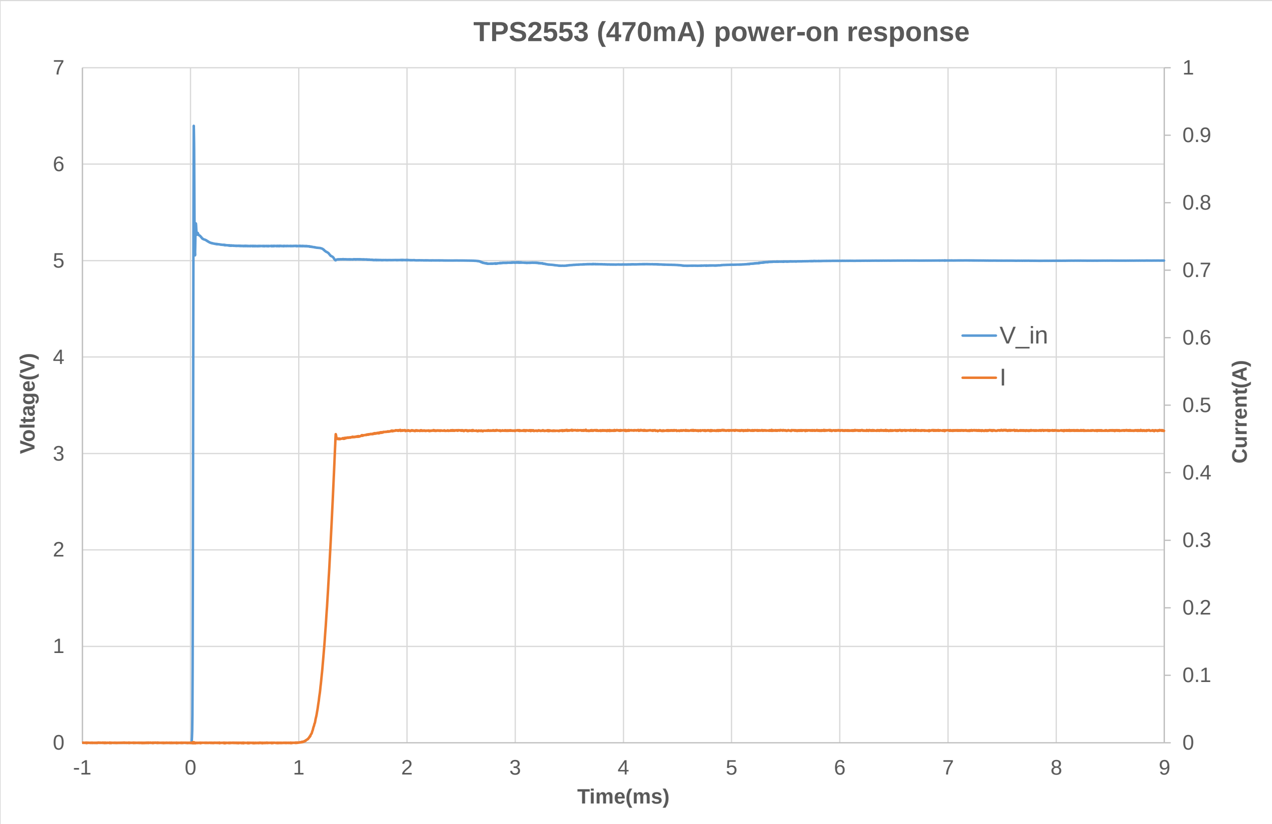

Figure 16: power-on response of the test circuit

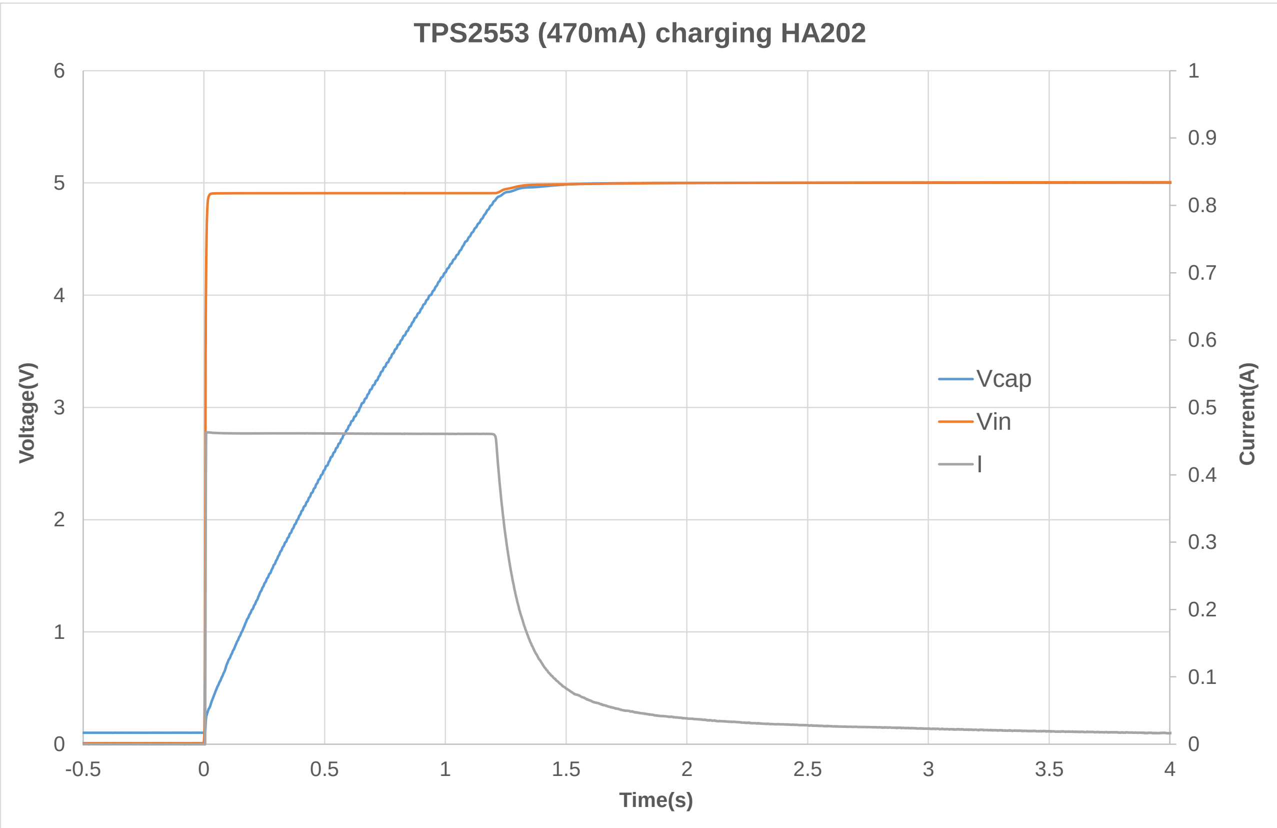

Figure 17: test circuit charging a HA202 (120mF)

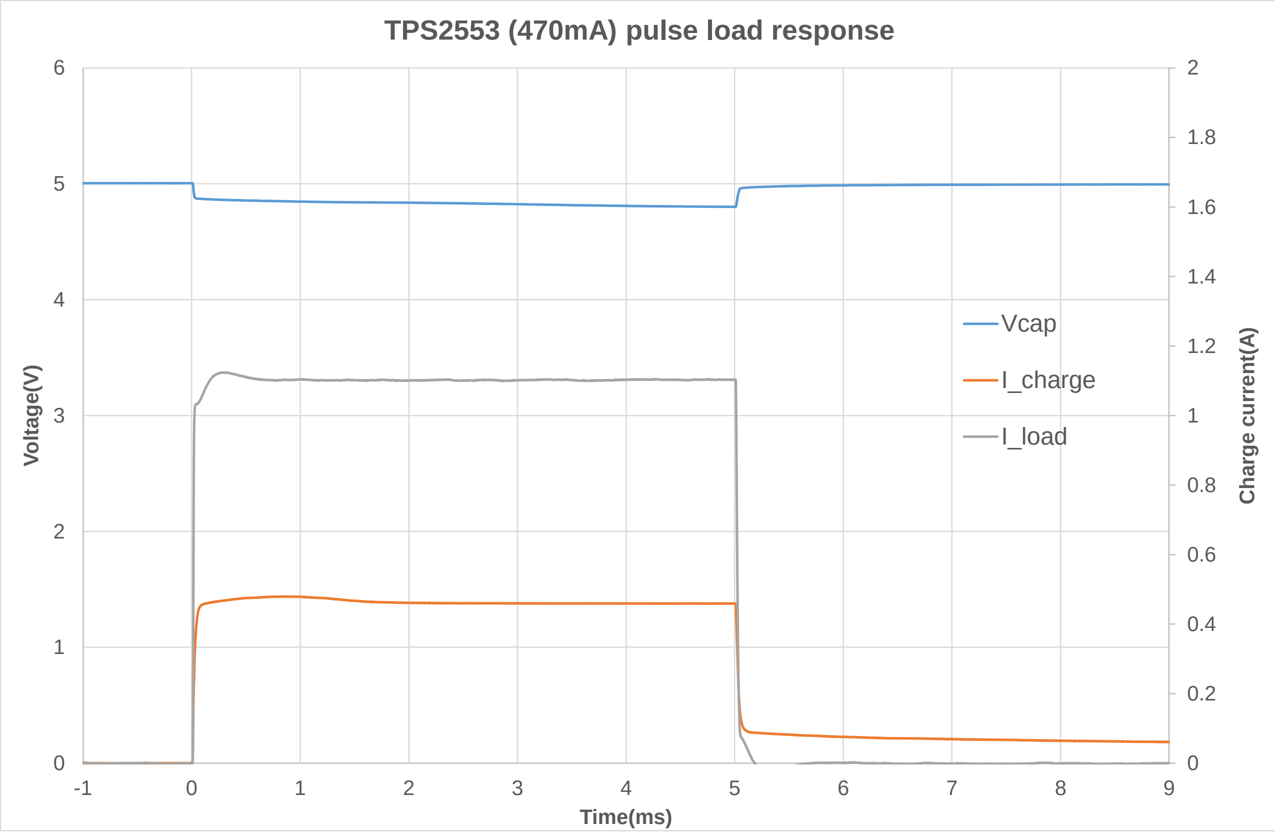

Figure 18: test circuit pulse load response with HA202(120mF)

Many other current limit power distribution switches would work. Below are some examples offered by various manufacturers.

Recommended parts:

Part number	Package	Current limit range	Operating voltage
LM3525	SOIC-8	0.5 - 1.5A	2.7V – 5.5V
TPS2553D	SOT23-6	0.075 - 1.5A	2.7V – 5.5V
NCP380	SOIC-8/MLP3X3	0.4 - 2A	2.8V – 36V
MAX891L	8 µMAX	0 - 0.5A	3V – 5.5V

Advantages:

- Small, simple, lower cost than discrete Op Amp current limit
- Adjustable current limit
- Thermal protection
- ENABLE input
- Reverse current blocking
- Fault detection

Disadvantages:

- Higher cost than the solutions using 2 x PFETs
- Small package limits power dissipation
- Most won't work at single cell voltage, <2.7V
- Linear current limit - wasteful of energy

General Purpose Evaluation Board

CAP-XX has available a general purpose evaluation board with various current limit options and cell balancing options to accelerate development of your supercapacitor circuit, refer to User Manual for APPEB1002 Supercapacitor Eval Board. It can be purchased from the CAP-XX website.

Further Information

CAP-XX will be pleased to provide further information on the applications described here, and on the use of supercapacitors in any application. Please use the contact details provided on the CAP-XX web site (https://www.cap-xx.com).

This application white paper is available on the CAP-XX web site. On the web site you may also find product bulletins, datasheets, SPICE models, application white papers, application briefs and design-aid calculators.