

DATASHEET

HY SERIES RADIAL LEAD SUPERCAPACITOR

Revision 3.3, Sept 2022

The HY series of supercapacitors are high temperature (85°C) cylindrical cells offering excellent value. They are available as single cells, or dual cell modules with a choice of cell balancing options.

Features:

- High power output to support peak current loads
- On-board energy storage to handle power surges (high capacitance and energy density)
- Long cycle life
- Wide temperature range (-40°C to +85°C)

Applications:

- Energy Harvesting for wireless sensors
- Peak power support for GSM/GPRS transmission
- Peak power support for low power batteries such as Lithium Thionyl Chloride batteries during automatic meter reading data transmission and last gasp transmission at end of battery life
- Peak power support for locks & actuators
- Peak power support for portable drug delivery systems
- Short term bridging power for power interruptions or battery hot swap



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Electrical Specifications

Single cells

Part numbering code

H	Y	N	vvv	dd	lll	S	ccc	R
Model	Cylindrical	# of cells	Voltage	Diameter (mm)	Length (mm)	Tolerance	Capacitance (μ F)	Lead format
High temp		1	2R7 = 2.7V	6C = 6.3 08 = 8.0 10 = 10 1B = 12.5 16 = 16 18 = 18	012 = 12 040 = 40	M \pm 20% S +50% /-20% V +30% /-10%	Two digits + number of zeros. 155 = 1500000 μ F = 1.5F	R = radial

Rated Voltage: 2.7V

Temperature Range: -40°C to +85°C

Parameters measured at 25°C

CAP-XX Part no.	Cap (F)	DC ESR Max (m Ω)	IL max @ 72 Hrs (μ A)	Diameter (mm)	Length (mm)	Mass (gm)
HY12R76C012V105R	1	210	2	6.3	12	0.7
HY12R708012S105R	1	210	2	8	12	0.9
HY12R708014V205R	2	140	4	8	14	1.2
HY12R708020V335R	3.3	110	7	8	20	1.4
HY12R708014V335R	3.3	140	7	8	14	1.3
HY12R708024V505R	5	85	10	8	24	1.7
HY12R710020S505R	5	50	10	10	20	2.3
HY12R710020V705R	7	50	14	10	20	2.3
HY12R710025V106R	10	45	20	10	25	2.7
HY12R71B020V106R	10	40	20	12.5	20	3.4
HY12R71B020V126R	12	40	28	12.5	20	3.4
HY12R71B025V156R	15	50	35	12.5	25	4.3
HY12R71B030V206R	20	40	47	12.5	30	5.2
HY12R71B034V206R	20	40	47	12.5	34	5.6
HY12R716025V256R	25	40	75	16	25	7.4
HY12R718040V506R	50	35	150	18	40	13.8

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Dual Cell Modules

Part numbering code

H	Y	N	vvv	tt	ll	S	ccc	R	B
Model	Cylindrical	# of cells	Voltage	Module thickness (mm)	Length (mm)	Tolerance	Cap. (µF)	Lead & package format	Balancing
High Temp		2	5R5 = 5.5V	8E = 8.5 11 = 11	13 = 13 37 = 37	M ± 20% S +50% /-20% V +30% /-10%	Two digits + number of zeros.	R = shrink wrap – see dwg	R = Resistor ¹ A = Active ²

Notes:

1. R means that a pair of 220KΩ, size 0402 balancing resistors are used.
2. A means that the CAP-XX active balancing circuit which draws < 1µA is used.

Rated Voltage: 5.5V

Temperature Range: -40°C to +85°C

Parameters measured at 25°C

CAP-XX Part no. ¹	Cap (F)	DC ESR Max (mΩ)	IL max ² @ 72 Hrs (µA) with resistor balance B=R	IL max ³ @ 72 Hrs (µA) with active balance B=A	Thick x Width (mm)	Length (mm)
HY25R50713V474RR	0.47	420	15	3	7x13	13
HY25R58E13S504RR	0.5	420	15	3	8.5x17	13
HY25R58E13V105RR	1	420	17	5	8.5x17	13
HY25R58E22V155RR	1.5	225	19	7	8.5x17	22
HY25R58E16V155RR	1.5	280	19	7	8.5x17	16
HY25R58E26V255RR	2.5	170	23	11	8.5x17	26
HY25R51122S255RR	2.5	100	23	11	11x21	22
HY25R51122V355RR	3.5	100	27	15	11x21	22
HY25R51127V505RR	5	90	33	21	11x21	27
HY25R51322V505RR	5	85	33	21	13x26	22
HY25R51327V755RR	7.5	100	43	31	13x26	27
HY25R51332V106RR	10	80	53	41	13x26	32
HY25R51336V106RR	10	85	53	41	13x26	36
HY25R51727V126RR	12.5	80	63	51	17x33	27
HY25R51942V256RR	25	70	113	101	19x37	42

Notes:

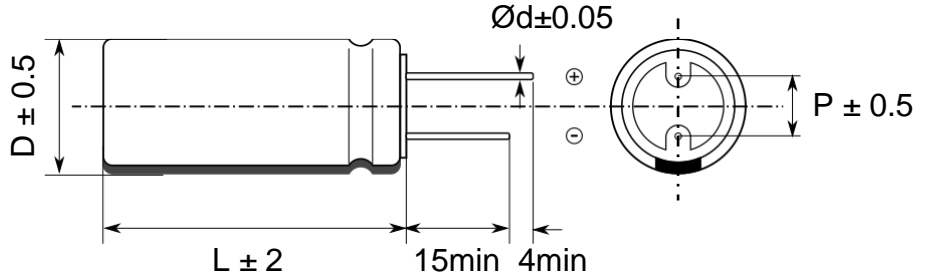
1. For a possible module consisting of 2 single cells listed on page 2, but not shown in the table above, please contact CAP-XX.
2. Includes balancing current through 220KΩ resistors at 2.75V/cell. If cell voltage is reduced, e.g. 1.8V/cell, then balancing current is reduced by $(2.75V-1.8V)/220K\Omega = 4\mu A$, so for example, the leakage current with balancing resistors for the HY25R50713V474RR at 3.6V would reduce from 15µA to 11µA.
If a different value of balancing resistor is desired, please contact CAP-XX.
3. Cell leakage current + 1µA for the active balance circuit.

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Dimensions (all units in mm)

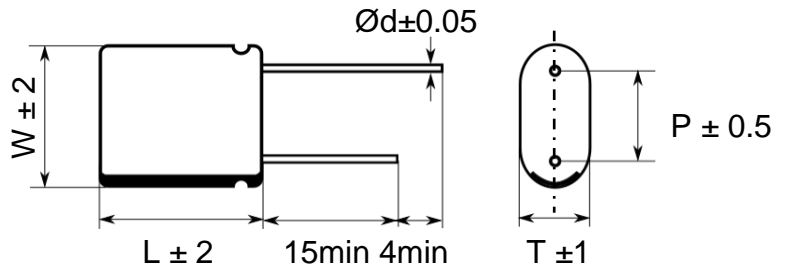
HY1 Series Shrink Wrap Radial Lead 1F – 50F

ΦD	P	Φd
6.3	2.5	0.5
8	3.5	0.6
10	5	0.6
12.5	5	0.6
16	7.5	0.8
18	7.5	0.8



HY2 Series Shrink Wrap, 0.47F – 25F

Cell dia.	T	W	P	Φd
6.3	7	13	8.8	0.5
8	8.5	17	12	0.6
10	11	21	15.5	0.6
12.5	13	26	18	0.6
16	17	33	24	0.8
18	19	37	26	0.8



Measurement of capacitance

Capacitance is measured at 25°C using the method specified by IEC62391 shown in Fig 1. This measures DC capacitance. The capacitor is charged to rated voltage, V_R , at constant current, held at rated voltage for at least 30 minutes and then discharged at constant current. The time taken to discharge from $0.8 \times V_R$ to $0.4 \times V_R$ is measured to calculate capacitance as:

$$C = I \times (T_1 - T_2) / (V_1 - V_2)$$

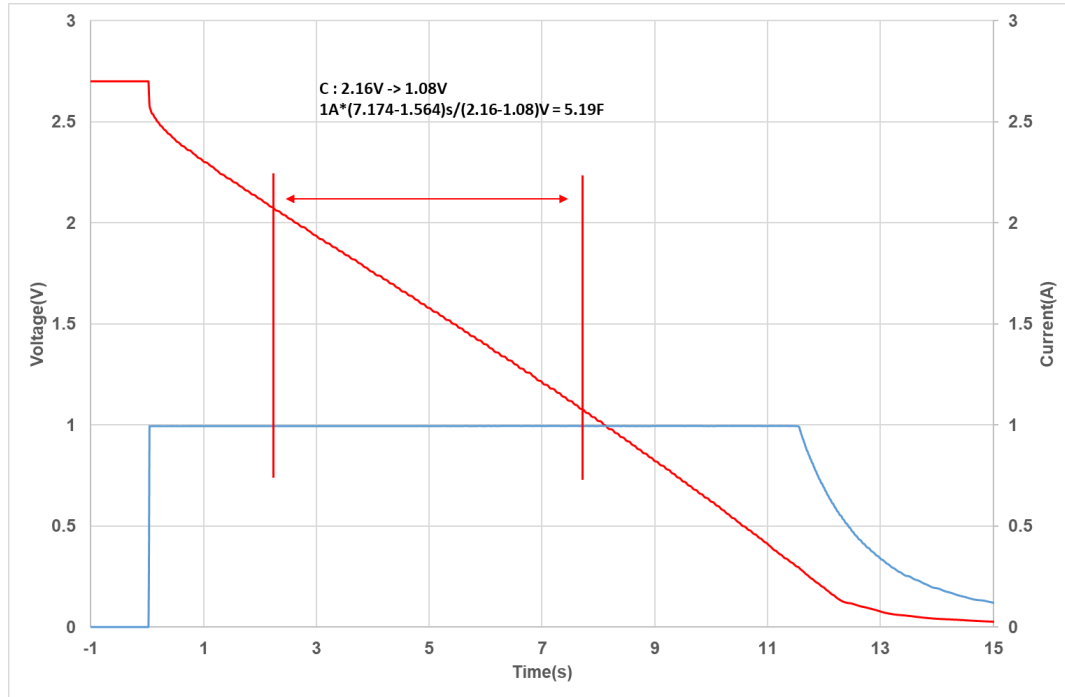


Fig 1: HY12R708024V505R Capacitance measurement

In this case, $C = 1A \times (7.174 - 1.564)s / (2.16 - 1.08)V = 5.19F$, which is well within the $5F +30\% / - 10\%$ tolerance for a HY12R708024V505R cell.

Measurement of ESR

Equivalent Series Resistance (ESR) is measured at 25°C by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 200µs after the step current is applied to ensure the voltage and current have settled. In this case, for a HY12R708024V505R the ESR is measured as $94\text{mV}/1.2\text{A} = 78.3\text{m}\Omega$, less than the 85mΩ maximum specified.

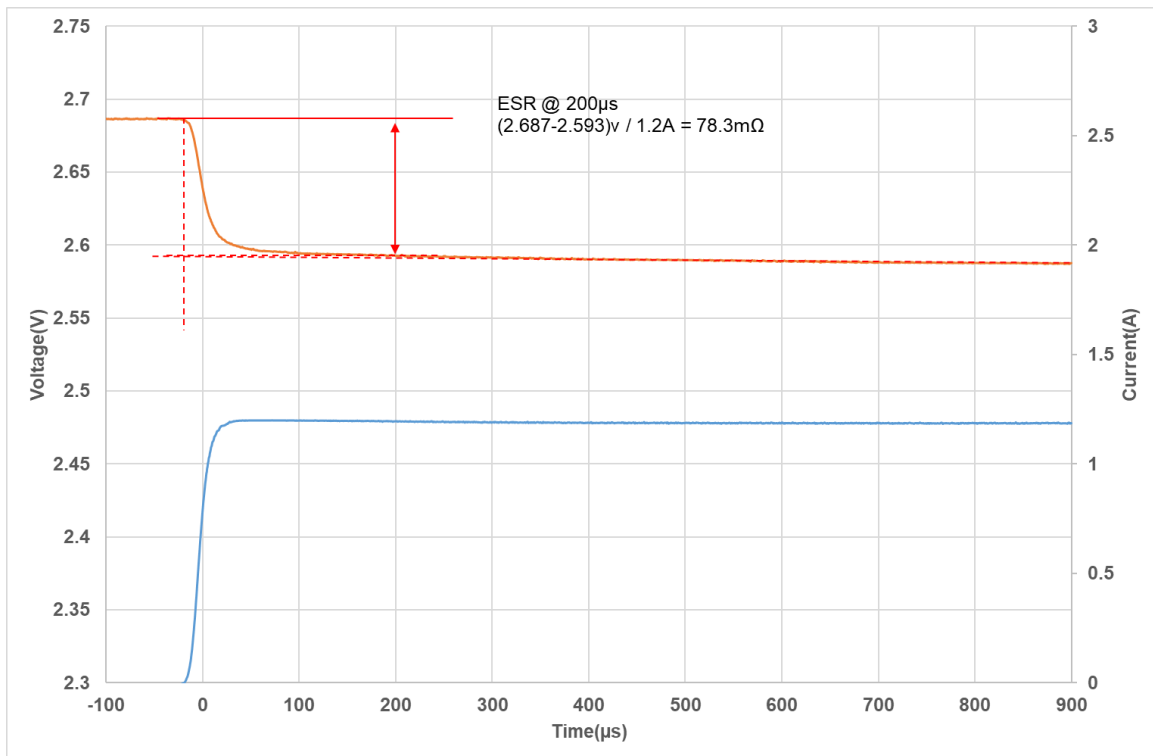


Fig 2: HY12R708024V505R ESR Measurement

Measurement of Leakage Current

Leakage current is measured by holding the supercapacitor at rated voltage at 25°C and measuring the current drawn through a high value resistor, typically 1KΩ or 2.2KΩ. The leakage current decays over time as shown in Fig 3 which shows the average leakage current for HY series supercapacitors. Fig3 shows that the long-term equilibrium leakage current is typically < 1μA/F but the datasheet quotes the maximum values after 72hrs at rated voltage.

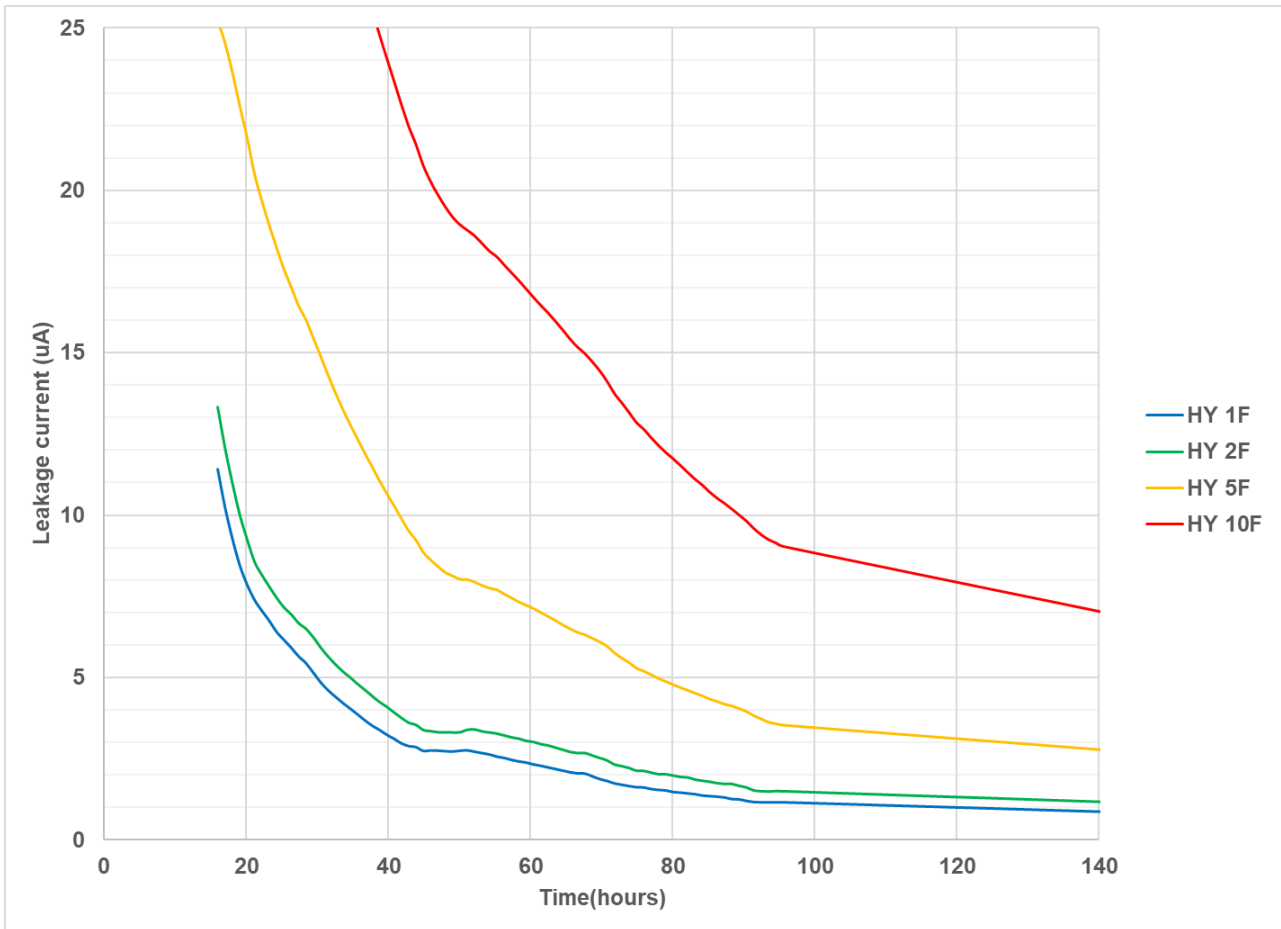


Fig 3: Leakage current measurement

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Variation in DC Capacitance and ESR with temperature

Figure 4 shows that DC capacitance does not vary with significantly over the operating temperature range of -40°C to +85°C.

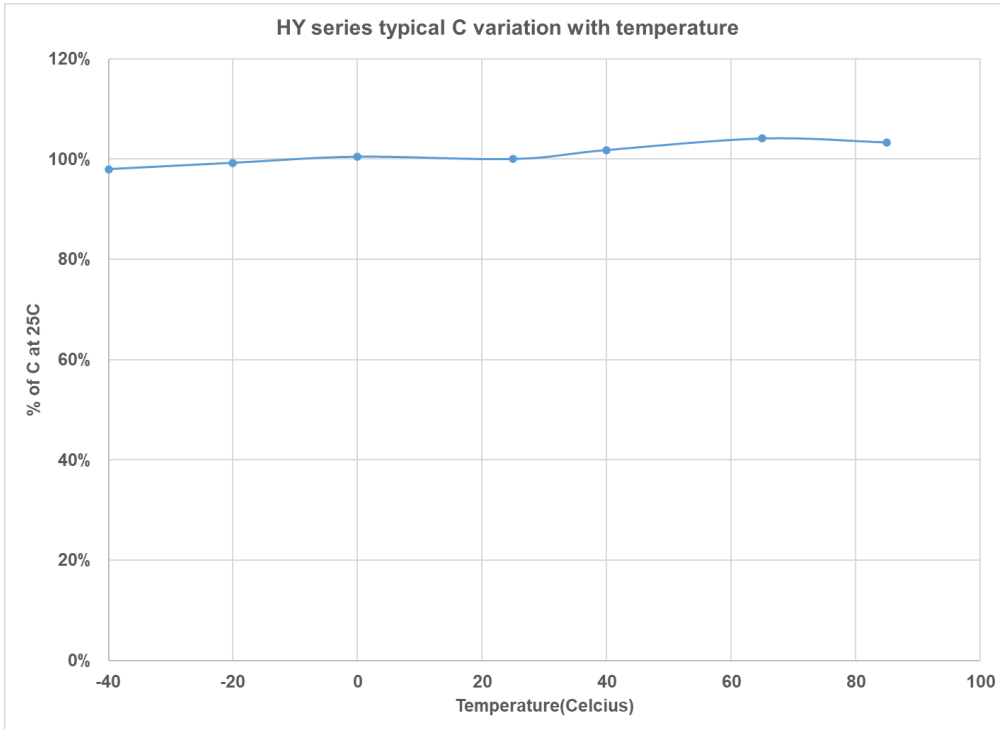


Fig 4: Typical variation in DC Capacitance over the operating temperature range

Figure 5 shows variation in DC ESR over the operating temperature range.

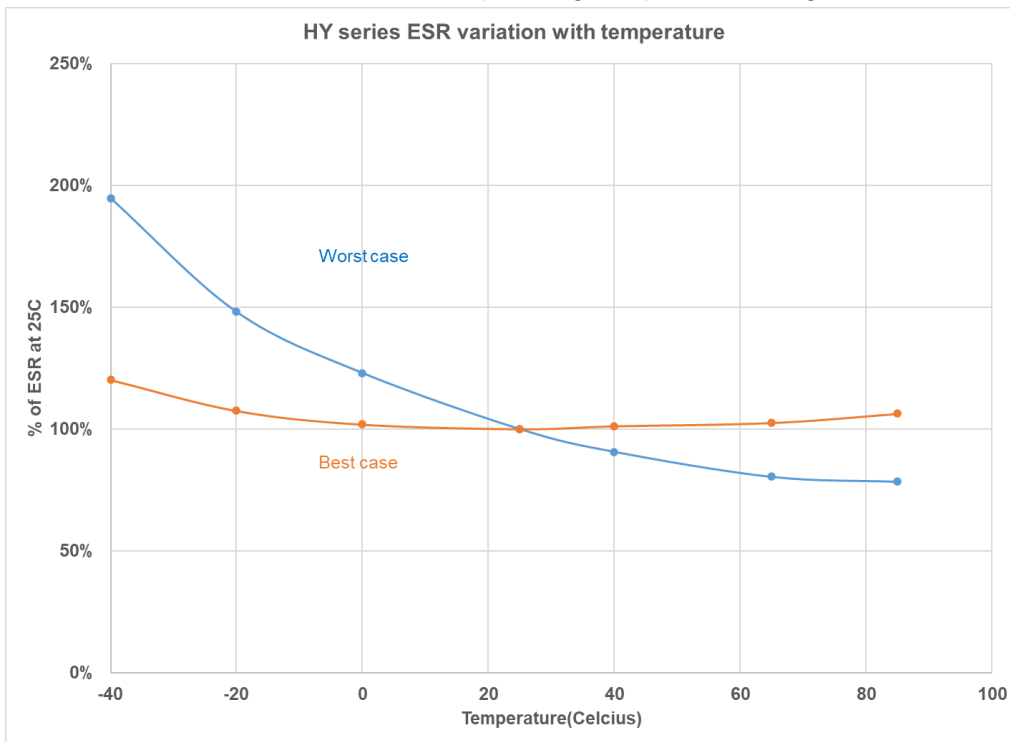


Fig 5: Typical variation in DC ESR over the operating temperature range

From Figure 5, ESR_{DC} at -40°C varies from ~1.2 to 1.9 x ESR_{DC} at room temperature. ESR_{DC} at 85°C is 70% to 105% of ESR_{DC} at room temperature. The variation in ESR with temperature is due to the change in the mobility of ions in solution in the electrolyte.

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Peak Current

Peak current is limited by $V_{rated}/(ESR + R_L)$ where R_L is the load resistance including parasitic resistance such as PCB traces. The current then decays and is given by:

$$[V_{rated}/(ESR + R_L)].e^{-t/[(ESR+R_L).C]}$$

where t = time in seconds. At high peak current, the supercapacitor discharges rapidly so that self heating due to the high current is negligible. Table 1 Shows short circuit current for a range of supercapacitors initially charged to 2.7V at the instant the short circuit is applied and after 100ms. It also shows the temperature increase recorded due to the short circuit.

Table 1:

Capacitance (F)	Instantaneous peak current (A)	Current after 100ms (A)	Temperature rise (°C)
10	92	49	3
5	80	38	2.1
2	36	14	1.3
1	28	9	1

In all cases the temperature rise is not significant. A one-time peak current pulse is only limited by the $ESR_{DC} + \text{Load resistance}$, not by any thermal limitations.

The voltage drop when a constant current pulse of duration τ is applied =

$$V_{INIT} - V_{FINAL} = I.ESR_{DC} + I.\tau/C$$

Where:

I = constant current

τ = duration of constant current

V_{INIT} = the initial voltage when the current pulse is first applied

V_{FINAL} = the supercapacitor voltage at the end of the pulse

Re-arranging terms, the maximum current that can be sustained for a time τ , when the supercapacitor is initially charged to rated voltage, V_R , and discharged to V_{MIN} , the minimum voltage that supports the given application =

$$I_{MAX} = \frac{V_R - V_{MIN}}{ESR_{DC} + \frac{\tau}{C}}$$

Maximum Continuous Current

Continuous current flow into/out of the supercapacitor will cause self-heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, and then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 6 shows the increase in temperature above ambient temperature as a function of RMS current for various supercapacitors.

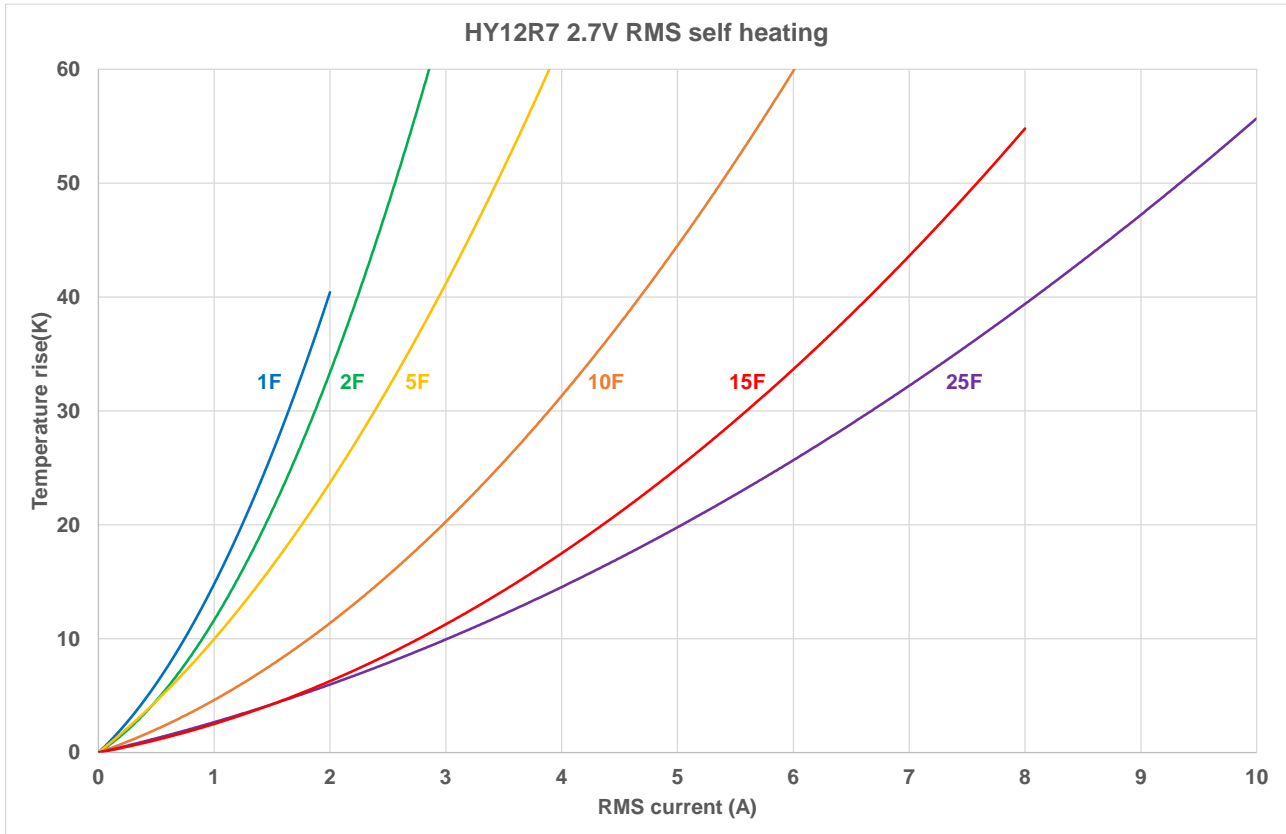


Fig 6: Self heating with RMS current for HY series supercapacitors

From Fig 6, the maximum RMS current in an application can be calculated. For example, if the ambient temperature is 40°C, and the maximum operating temperature for the supercapacitor is 85°C, then the maximum RMS current for a 10F supercapacitor should be limited to 5A, which causes a 45°C temperature increase.

Effective capacitance (Ceff)

Effective capacitance is the capacitance seen for short pulse widths. Due to a supercapacitor's frequency response, for shorter pulse widths there will be less capacitance available than the DC capacitance. In Fig 7, consider the voltage drop due to capacitance after 10ms = 2.662V – 2.654V = 8mV. Therefore $C_{eff}(10ms) = \text{Discharge_Current} \times 10ms / \text{Voltage_drop}(10ms) = 1.05A \times 0.01s / 0.008V = 1.3F$. The voltage drop due to capacitance after 100ms = 2.662V – 2.636V = 26mV, hence $C_{eff}(100ms) = 1.05A \times 0.1s / 0.026V = 4.0F$. Fig 8 shows C_{eff} as a % of DC capacitance for the HY series of supercapacitors.

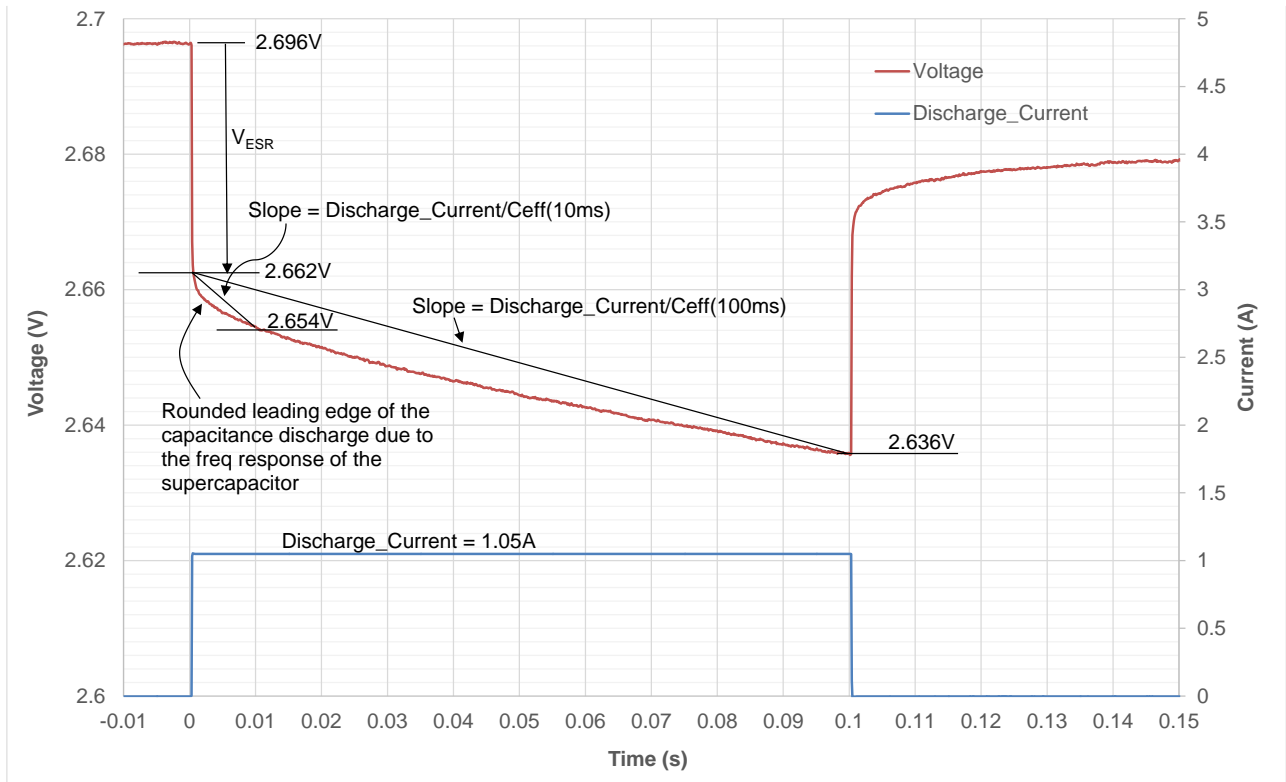


Fig 7: Discharge pulse illustrating the concept of Ceff

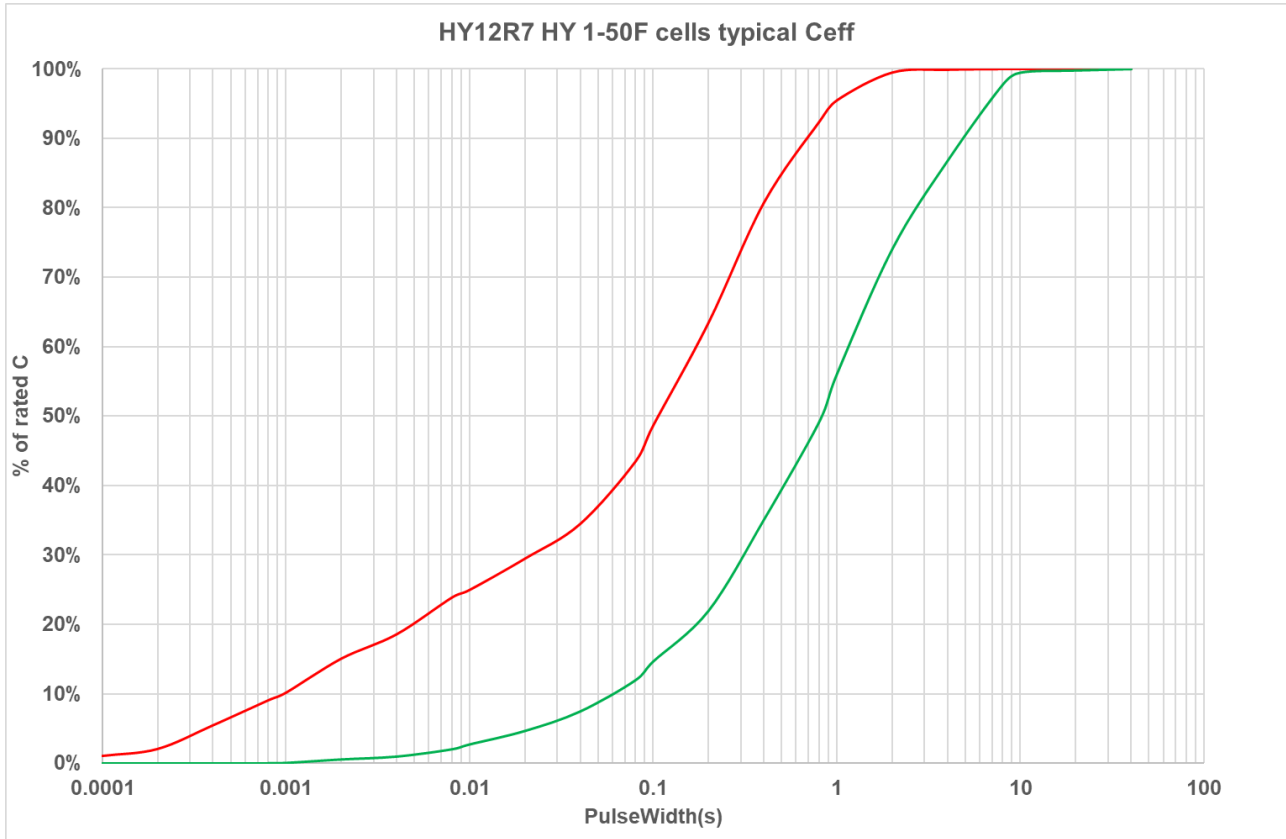


Fig 8: Typical range of effective capacitance for HY 2.7V series supercapacitors

For any given pulse width, T, with a constant discharge current I_{DISCH} , the voltage drop is given by:

$$V_{drop} = I_{DISCH} \times ESR + I_{DISCH} \times T/C_{eff}(T)$$

Where $C_{eff}(T) = DC \text{ capacitance} \times \% \text{ at time } T \text{ read from Fig 8.}$

Shorter pulses need less capacitance to support them, so the supercapacitors can support short pulses despite their frequency response.

Balancing options

In many applications a voltage $> 2.7V$ but $\leq 5.5V$ is required. For these applications 2 supercapacitor cells are connected in series in dual cell modules such as the CAP-XX HY2 series which is rated to 5.5V. These cells should have a balancing circuit to ensure that the cell voltages remain approximately equal or the cell with the lower C will have a higher voltage across it, causing it to age faster than its companion cell, hence losing even more C until it goes over voltage. This is a reason why a balancing circuit should aim to maintain the voltage across each cell equal, rather than just prevent over-voltage. As an example, if the dual cell module was at 5.0V and there were over-voltage protection circuits that prevented each cell from exceeding 2.7V, then module could have one cell at 2.7V and the other at 2.3V. The cell at 2.7V will age faster than the cell at 2.3V and will age faster than if both cells were held at 2.5V shortening module life.

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In the HY2 series modules there is a PCB connecting the 2 cells. This PCB can have one of two balancing options:

1. Option “R” as the last character in the HY2 series part number.
A pair of balancing resistors are fitted, one resistor across each cell. The balancing resistors increase leakage current drawn by the module. CAP-XX uses 220K Ω balancing resistors which adds 12.5 μ A leakage current at 5.5V or 8.2 μ A at 3.6V.
2. Option “A” as the last character in the HY2 series part number.
An op amp maintains the midpoint voltage = $\frac{1}{2}$ the supercapacitor module terminal voltage. This solution maintains the midpoint voltage very accurately, responds more quickly than balancing resistors as the supercapacitor charges and discharges and only adds \sim 1 μ A to leakage current.
This option is only available as a special order. Minimum order quantity will apply.

If the application uses a supercapacitor charging IC that has an integrated supercapacitor midpoint balancing circuit, or there is a balancing circuit on the PCB, then order 2 x HY1 cells and place them in series. This makes the midpoint available to your balancing circuit. The dimensions of 2 HY1 cells placed next to each other are the same as a shrink wrapped HY2 series cell, refer to Dimensions on page 4 of this datasheet. Refer to the Application Whitepaper on Supercapacitor Cell Balancing under the DESIGN AIDS section of the CAP-XX website, www.cap-xx.com for more information on cell balancing.

Storage

CAP-XX recommends storing supercapacitors in their original packaging in an air conditioned room, preferably at $< 30^{\circ}\text{C}$ and $< 50\%$ relative humidity. CAP-XX supercapacitors can be stored at any temperature not exceeding their maximum operating temperature but storage at continuous high temperature and humidity is not recommended and will cause premature ageing.

Do not store supercapacitors in the following environments:

- High temperature / high humidity
- Direct sunlight
- In direct contact with water, salt, oil or other chemicals
- In direct contact with corrosive materials, acids, alkalis or toxic gases
- Dusty environment
- In environments subjected to shock and vibration

Soldering

When soldering it is important to not over-heat the supercapacitor to not adversely affect its performance. CAP-XX recommends that only the leads come in contact with solder and not the supercapacitor body.

Hand Soldering

Heat transfers from the leads into to the supercapacitor body, so the soldering iron temperature should be $< 350^{\circ}\text{C}$ soldering time should be kept to the minimum possible and be less than 4 seconds.

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Wave Soldering

The PCB should be pre-heated only from the bottom and for < 60 secs with temperature $\leq 100^{\circ}\text{C}$ on the top side of the board for PCBs $\geq 0.8\text{mm}$ thick. The table below lists suggested solder temperatures.

Solder temperature $^{\circ}\text{C}$	Suggested solder time (s)
220	7
240	7
250	5
260	3

Reflow Soldering

Infrared or conveyor oven soldering techniques can be used providing the supercapacitor body is not subject to temperatures $> 85^{\circ}\text{C}$. Do not use a standard reflow oven.

Transportation

All the supercapacitor cells in this datasheet store $< 0.3\text{Wh}$ energy. The energy in watt-hours is calculated as: $\frac{1}{2} \times \text{Capacitance} \times V_{\text{rated}}^2 / 3600$. The largest cell in this range is 50F, so stored energy = $\frac{1}{2} \times 50 \times 2.7^2 / 3600 = 0.0506\text{Wh}$. Under regulation UN3499 there is no restriction on shipping these supercapacitors. Their shipping description is "Electrical Capacitors" with harmonized shipping code 8532.29.0040.