DATASHEET

GY SERIES SUPERCAPACITOR

Revision 3.1, May 2021

The GY series of supercapacitors are cylindrical cells offering excellent value. They are available as single cells, or dual cell modules with a choice of cell balancing options.

Features:

- High power output to support peak current loads
- On-board energy storage to handle power surges (high capacitance and energy density)
- Long cycle life

Applications:

- Energy Harvesting for wireless sensors
- Peak power support for GSM/GPRS transmission
- Last gasp power for remote meter status transmission
- Peak power support for locks & actuators
- Peak power support for portable drug delivery systems
- Short term bridging power to ride through power Interruptions or for battery hot swap

Electrical Specifications

Single cells

Part numbering code

G	Y	N	vvv	dd	lll	S	ccc	R
Model	**Cylindrical**	**# of cells**	**Voltage**	**Diameter (mm)**	**Length (mm)**	**Tolerance**	**Capacitance (µF)**	**Lead format**
		1	2R7 = 2.7V	6C = 6.3 08 = 8.0 10 = 10 1B = 12.5 16 = 16 18 = 18	012 = 12 068 = 68 120 = 120	M ± 20% S +50% /-20% V +30% /-10%	Two digits + number of zeros. e.g. 155 = 1500000µF = 1.5F	R = radial S = 2 solder pins W = 4 Cu tabs

Rated Voltage: 2.7V
Temperature Range: -40°C to +65°C
Parameters measured at 25°C

CAP-XX Part no.	Cap (F)	ESR Max @ 1KHz (mΩ)	Diameter (mm)	Length (mm)	IL max @ 72 Hrs (µA)
GY12R708012V105R	1	200	8	12	8
GY12R708012V205R	2	150	8	12	8
GY12R708014V205R	2	130	8	14	10
GY12R708020V335R	3.3	80	8	20	14
GY12R708025V505R	5	70	8	25	16
GY12R710020V505R	5	70	10	20	16
GY12R710020V705R	7	60	10	20	20
GY12R710025V106R	10	55	10	25	30
GY12R71B020V106R	10	50	12.5	20	30
GY12R71B025V156R	15	35	12.5	25	45
GY12R71B030V206R	20	40	12.5	30	60
GY12R716020V206R	20	30	16	20	60
GY12R716026V256R	25	25	16	26	80
GY12R716032V306R	30	22	16	32	100
GY12R716035V406R	40	16	16	35	120
GY12R718040V506R	50	15	18	40	140
GY12R718040V606R	60	15	18	40	140
GY12R718050V706R	70	14	18	50	160
GY12R718060V107R	100	12	18	60	180
GY12R722045V107R	100	12	22	45	180

Dual Cell Modules

Part numbering code

G	Y	N	vvv	tt	ll	S	ccc	R	B
Model	**Cylindrical**	**# of cells**	**Voltage**	**Module thickness (mm)**	**Length (mm)**	**Tolerance**	**Cap. (µF)**	**Lead & package format**	**Balancing**
		2	5R5 = 5.5V	8E = 8.5 11 = 11 13 = 13 17 = 17	17 = 17 44 = 44	M ± 20% S +50% /-20% V +30% /-10%	Two digits + number of zeros.	R= shrink wrap, radial leads – see dwg P = plastic, radial leads – see dwg	R = Resistor* A = Active*

*R pair of balancing resistors, 0402 resistors, nominal value stated in table below
*A = CAP-XX active balancing circuit which draws < 1µA.

Rated Voltage: 5.5V
Temperature Range: -40°C to +65°C
Parameters measured at 25°C

Shrink Wrap

CAP-XX Part no.	Cap (F)	ESR Max @ 1KHz (mΩ)	Thick x Width (mm)	Length (mm)	IL max @ 72 Hrs (µA) with active balance x=A	IL max @ 72 Hrs (µA) with resistor balance x=R	Nominal balancing resistor value (kΩ) x=R
GY25R58E17V504Rx	0.5	400	8.5 x 17	14	9	66	47
GY25R58E17V105Rx	1	260	8.5 x 17	17	11	68	47
GY25R58E23V155Rx	1.5	160	8.5 x 17	23	16	73	47
GY25R51123V255Rx	2.5	140	11 x 21	23	21	143	22
GY25R51121V355Rx	3.5	120	11 x 21	21	26	148	22
GY25R51127V505Rx	5	110	11 x 21	27	31	153	22
GY25R51327V505Rx	5	80	13 x 26	27	31	210	15
GY25R51327V755Rx	7.5	90	13 x 26	27	41	220	15
GY25R51628V126Rx	12.5	50	16 x 32	28	81	410	8.2
GY25R51842V256Rx	25	30	18 x 36	42	141	538	6.8

Plastic case

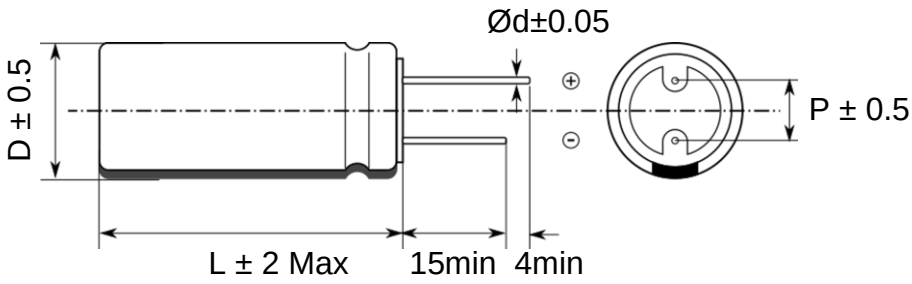
CAP-XX Part no.	Cap (F)	ESR Max @ 1KHz (mΩ)	Thick x Width (mm)	Length (mm)	IL max @ 72 Hrs (µA) with active balance x=A	IL max @ 72 Hrs (µA) with resistor balance x=R	Nominal balancing resistor value (kΩ) x=R
GY25R50916V504Px	0.5	340	9 x 18	16	9	66	47
GY25R50916V105Px	1	350	9 x 18	16	11	68	47
GY25R50920V105Px	1	200	9 x 18	20	11	68	47
GY25R50924V155Px	1.5	190	9 x 18	24	16	73	47
GY25R51125V355Px	3.5	120	11 x 23	25	26	148	22

Notes:
1. x = R (for passive balancing with 2 resistors) or A for active balancing using an op amp.
2. Lists the default value of balancing resistor for this module. Contact CAP-XX if a different value is desired.
3. For a possible module consisting of 2 single cells listed on page 2, but not shown in table above, please contact CAP-XX.

Dimensions (all units in mm)

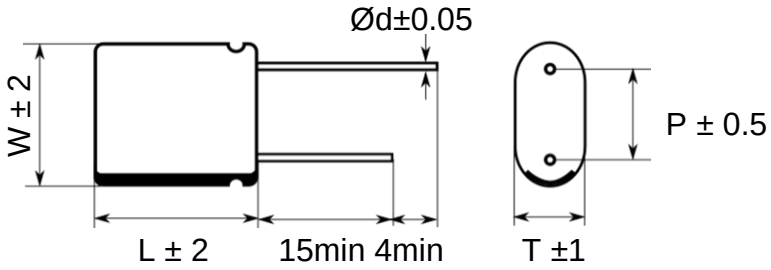
GY1 Series Shrink Wrap Radial Lead 1F – 100F

ΦD	P	Φd
6.3	2.3	0.6
8	3.5	0.6
10	5.5	0.6
12.5	5.5	0.6
16	8	0.8
18	8	0.8
22	10	1



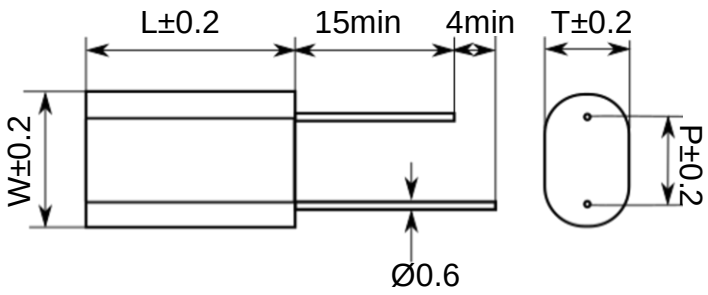
GY2 Series Shrink Wrap, 0.5F –25F; L = R

Cell dia.	T	W	P	Φd
8	8.5	17	11.5	0.6
10	11	22	15.5	0.6
12.5	13	25	18	0.6
16	17	32	24	0.8
18	19	36	26	0.8



GY2 Series Plastic Package, 0.5F – 3.5F; L = P

Cell dia.	T	W	P
8	9	18	11.5
10	11	23	15.5



Measurement of capacitance

Capacitance is measured at 25°C using the method specified by IEC62391 shown in Fig 1. This measures DC capacitance. The capacitor is charged to rated voltage, V_R, at constant current, held at rated voltage for at least 30 minutes and then discharged at constant current. The time taken to discharge from 0.8 x VR to 0.4 x VR is measured to calculate capacitance as:

$$C = I \times (T_1 - T_2)/(V_1 - V_2)$$

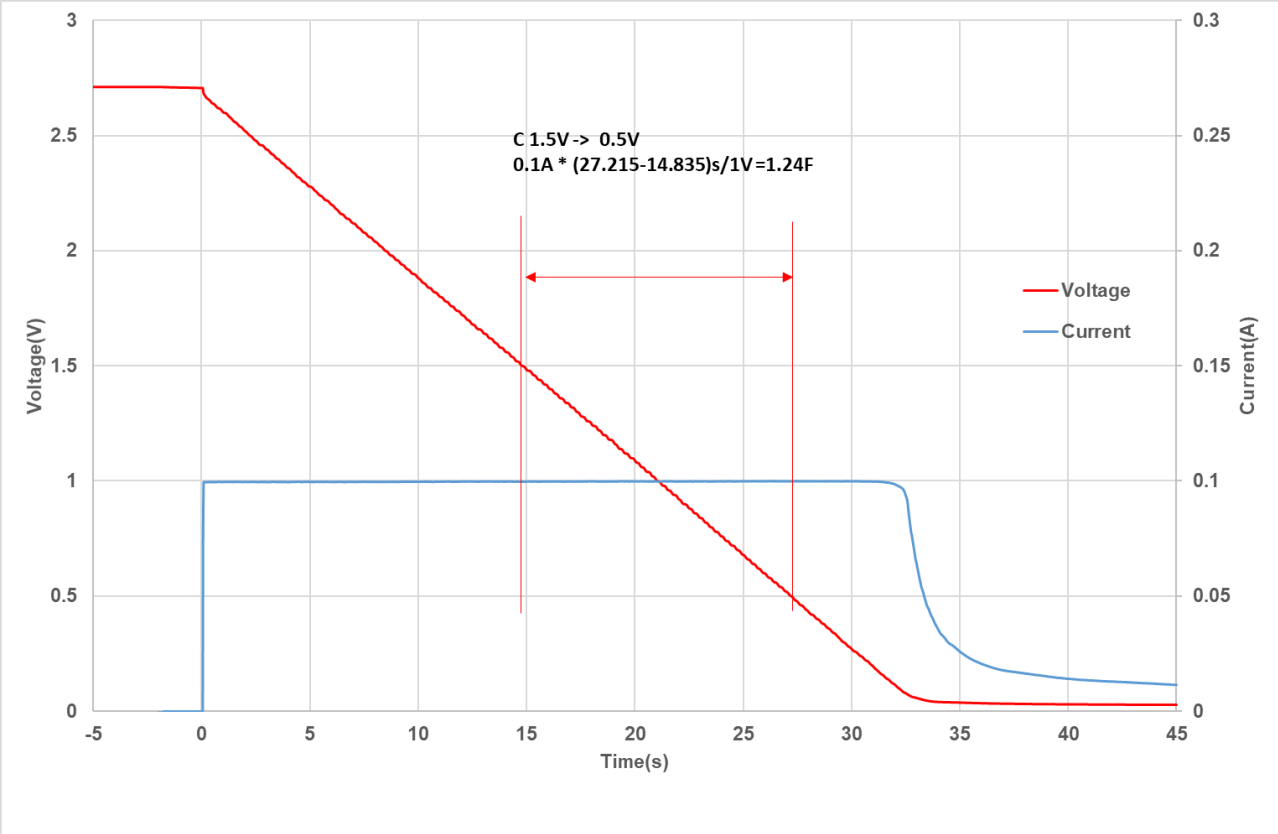


Fig 1: GY12R708012V105R Capacitance measurement

In this case, C = 0.1A x 12.38s /1V = 1.24F, which is well within the 1F +30% / - 10% tolerance for a GY12R708012V105R cell.

Measurement of ESR

Equivalent Series Resistance (ESR) is measured at 25°C by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 200µs after the step current is applied to ensure the voltage and current have settled. In this case, for a GY12R708012V105R the ESR is measured as 140mV/1A = 140mΩ.

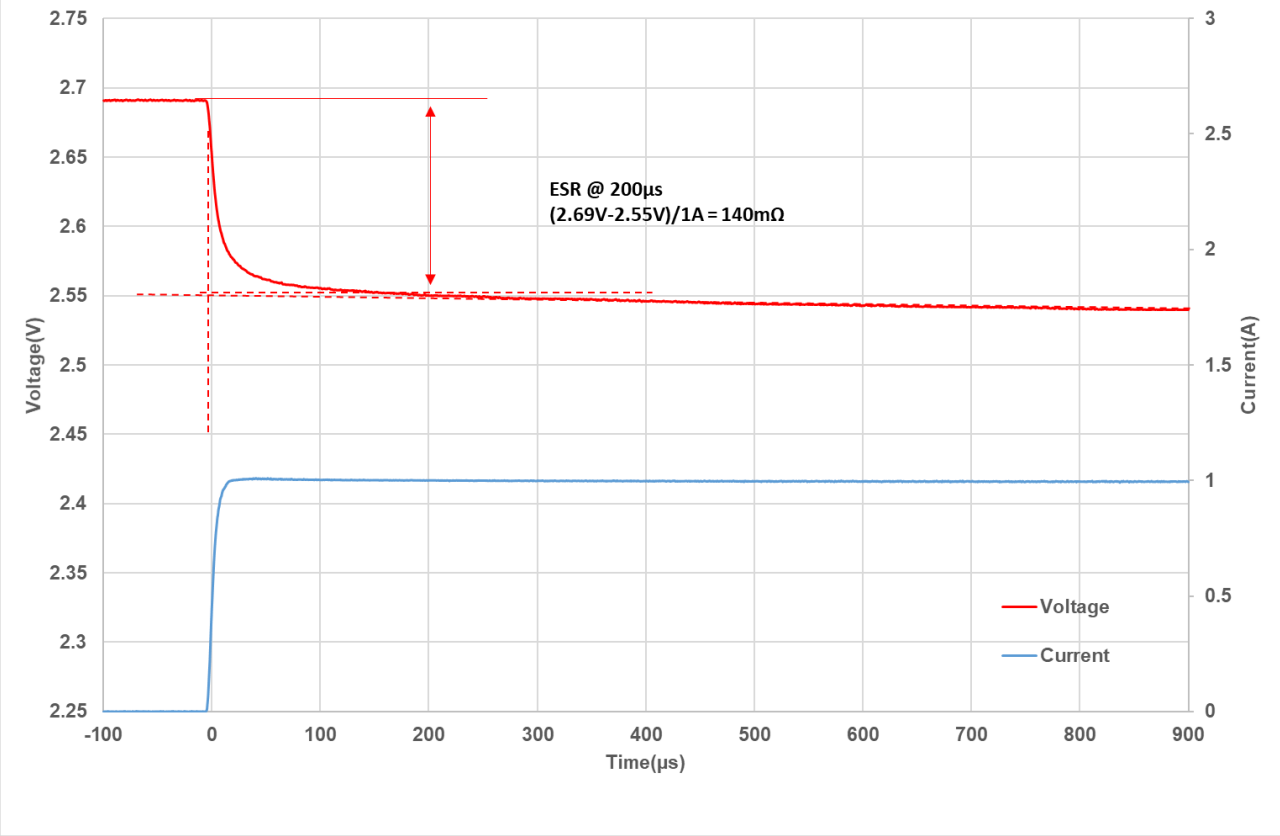


Fig 2: GY12R708012V105R ESR Measurement

Measurement of Leakage Current

Leakage current is measured by holding the supercapacitor at rated voltage at 25°C and charging it through a low value current limit resistor, in this case, 28Ω. After the current through the 28Ω resistor has decayed the supercapacitor is then held on charge with a higher value sense resistor, typically 1KΩ or 2.2KΩ, and measuring the voltage across this resistor to determine leakage current. The leakage current decays over time as shown in Fig 3 which shows the average leakage current for 4 samples each of 1F, 2F, 5F and 10F supercapacitors. Leakage current is typically 1.5µA/F but the datasheet quotes the maximum values. Leakage current in the datasheet is quoted after 72hrs at rated voltage.

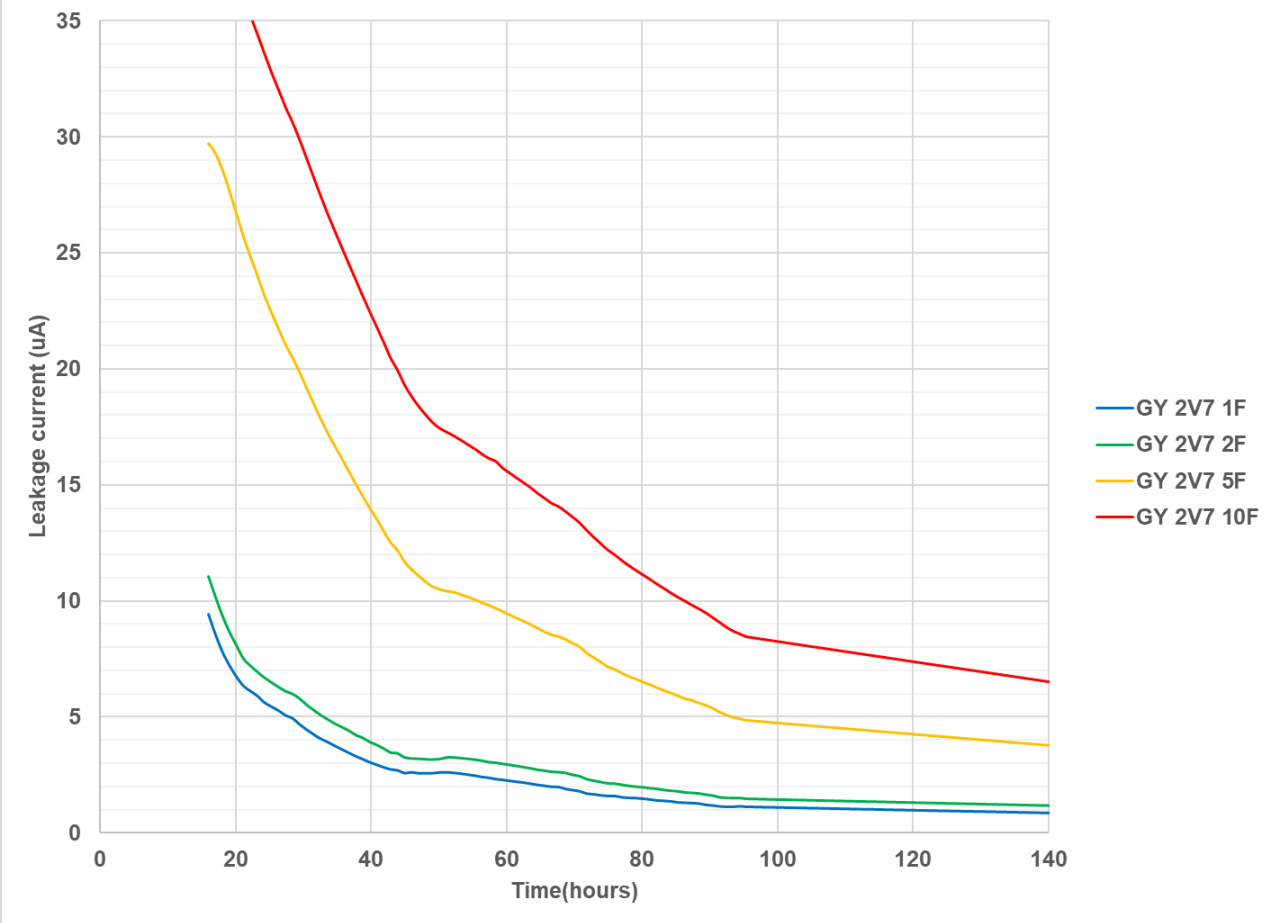


Fig 3: Leakage current measurement

Variation in DC Capacitance and ESR with temperature

Figure 4 shows that DC capacitance does not vary with significantly over the operating temperature range of -40°C to +65°C.

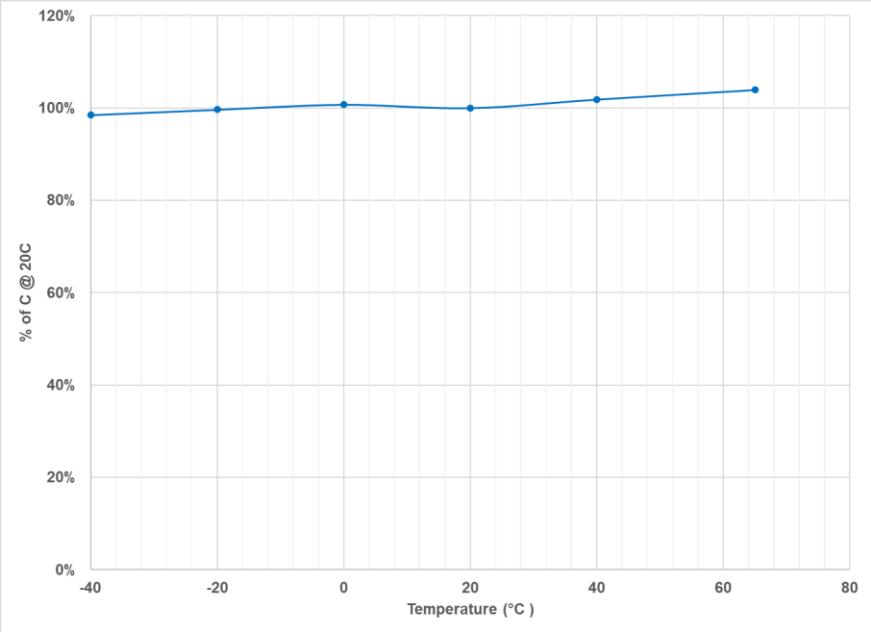


Fig 4: Typical variation in Capacitance over the operating temperature range

Figure 5 shows variation in DC ESR over the operating temperature range.

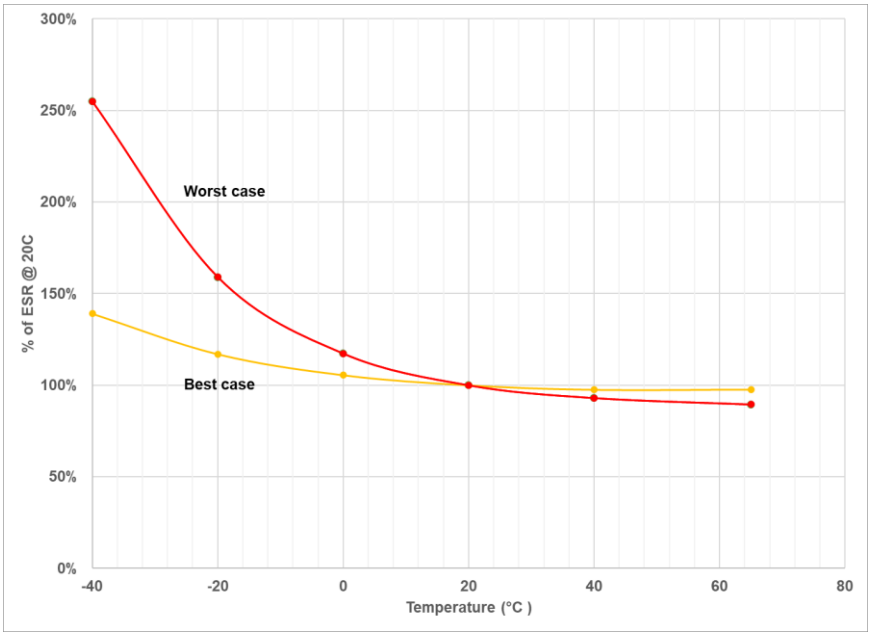


Fig 5: Typical variation in DC ESR over the operating temperature range

From Figure 5, ESR_{DC} at -40°C varies from ~2.6x to 1.4x ESR_{DC} at room temperature depending on the part. ESR_{DC} at 65°C is 80% to 100% of ESR_{DC} at room temperature. The variation in ESR with temperature is due to the change in the mobility of ions in solution in the electrolyte and the characteristics of the activated carbon used in that part.

Peak Current

Peak current is limited by Vrated/(ESR + R_L) where R_L is the load resistance including parasitic resistance such as PCB traces. The current then decays and is given by :

$$[Vrated/(ESR + R_L)].e^{-t/[(ESR+RL).C]}$$

where t = time in seconds. At high peak current, the supercapacitor discharges rapidly so that self heating due to the high current is negligible. Table 1 Shows short circuit current for a range of supercapacitors initially charged to 2.7V at the instant the short circuit is applied and after 100ms. It also shows the temperature increase recorded due to the short circuit.

Table 1:

Capacitance (F)	Instantaneous peak current (A)	Current after 100ms (A)	Temperature rise (°C)
10	78	40	3.7
5	51	30	2.6
2	35	14	1.6
1	28	9	1

In all cases the temperature rise is not significant. A one-time peak current pulse is only limited by the ESR_{DC} + Load resistance, not by any thermal limitations.
The voltage drop when a constant current pulse of duration τ is applied =

$$V_{INIT} - V_{FINAL} = I.ESR_{DC} + I.\tau/C$$

Where:

I = constant current
τ = duration of constant current
V_{INIT} = the initial voltage when the current pulse is first applied
V_{FINAL} = the supercap voltage at the end of the pulse

Re-arranging terms, the maximum current that can be sustained for a time τ, when the supercapacitor is initially charged to rated voltage, V_R, and discharged to V_{MIN}, the minimum voltage that supports the given application =

$$I_{MAX} = \frac{V_R - V_{MIN}}{ESR_{DC} + \frac{\tau}{C}}$$

Maximum Continuous Current

Continuous current flow into/out of the supercapacitor will cause self-heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, and then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 6 shows the increase in temperature as a function of RMS current for various GY12R7 series supercapacitors.

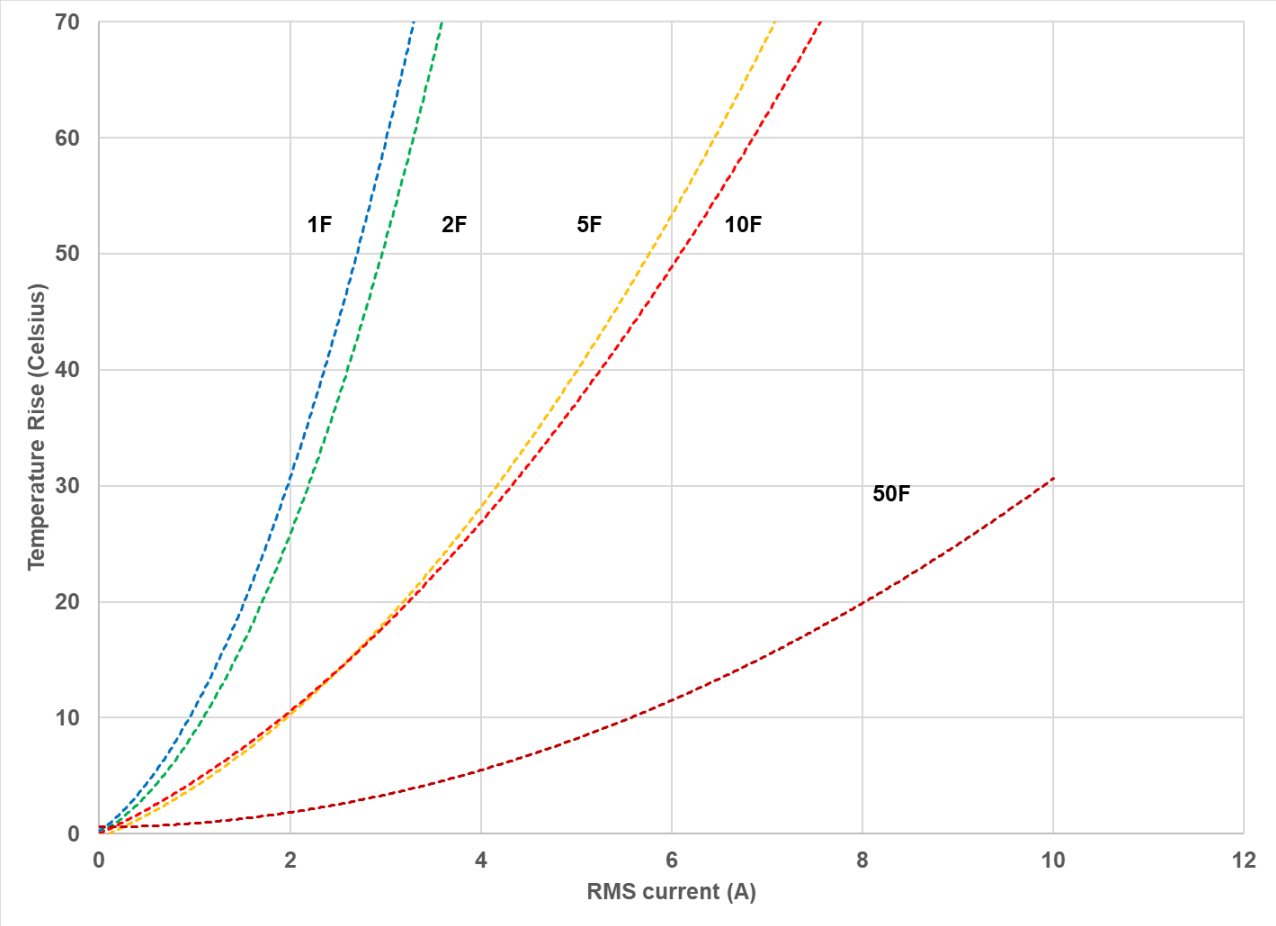


Fig 6: Self heating with RMS current for various supercapacitors

From Fig 6, the maximum RMS current in an application can be calculated. For example, if the ambient temperature is 40°C, and the maximum operating temperature for the supercapacitor is 65°C, then the maximum RMS current for a 10F supercapacitor should be limited to 3.8A, which causes a 25°C temperature increase.

Effective capacitance (Ceff)

Effective capacitance is the capacitance seen for short pulse widths. Due to the supercapacitor's frequency response, for shorter pulse widths there will be less capacitance available than the DC capacitance. In Fig 7, consider the voltage drop due to capacitance after 10ms = 2.662V – 2.654V = 8mV. Therefore Ceff(10ms) = Discharge_Current x 10ms/Voltage drop(10ms) = 1.05A x 0.01s/0.008V = 1.3F. The voltage drop due to capacitance after 100ms = 2.662V – 2.636V = 26mV, hence Ceff(100ms) = 1.05A x 0.1s/0.026V = 4.0F. Fig 8 shows Ceff as a % of DC capacitance for the GY series of supercapacitors.

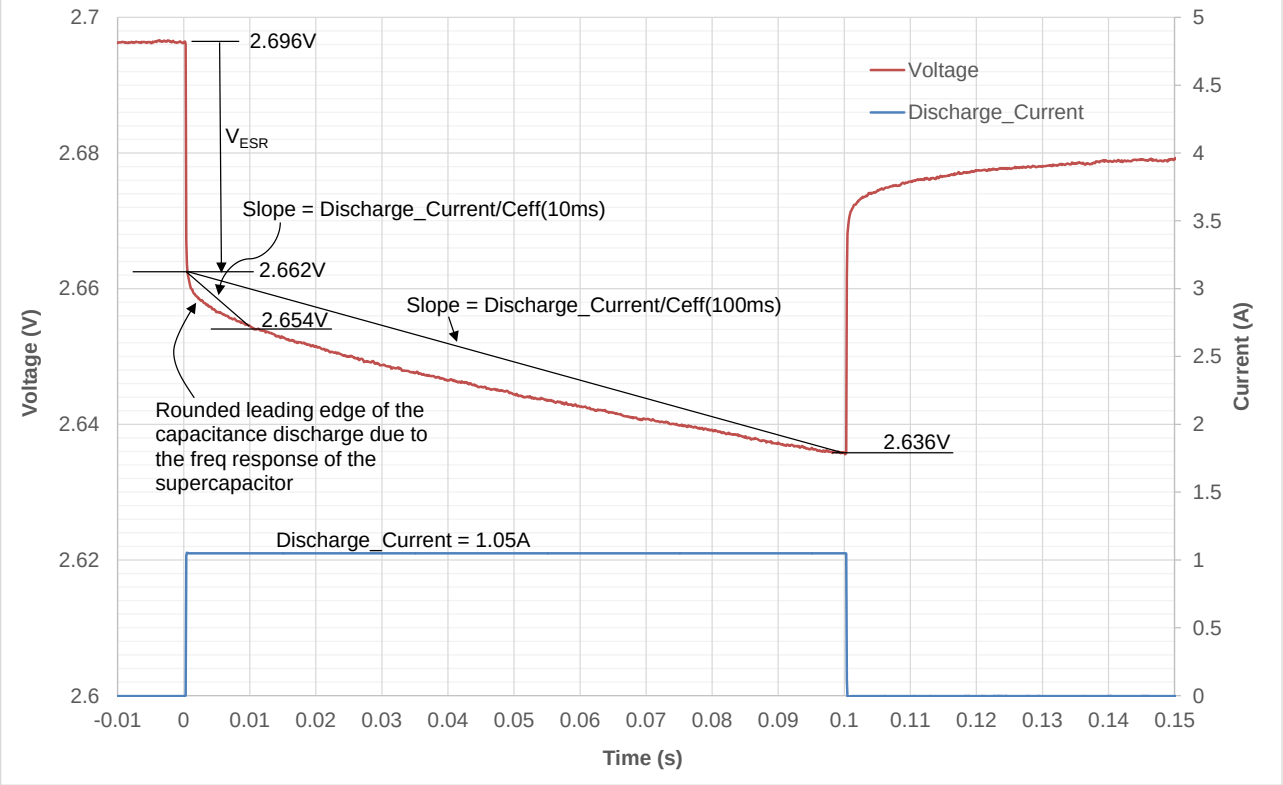


Fig 7: Discharge pulse illustrating the concept of Ceff

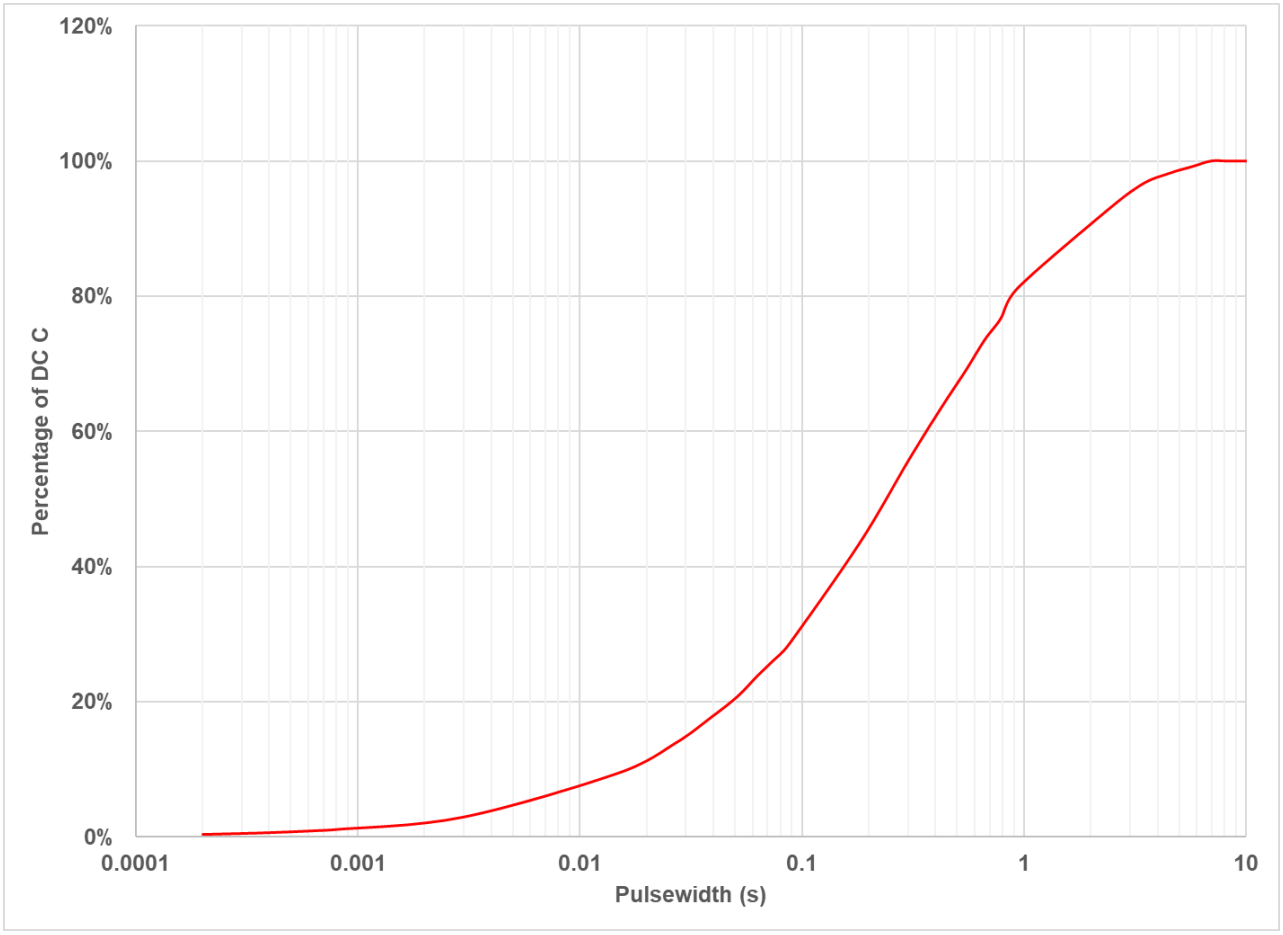


Fig 8: Typical effective capacitance for GY 2.7V series supercapacitors

For any given pulse width, T, with a constant discharge current I_{DISCH}, the voltage drop is given by:

Vdrop = I_{DISCH} x ESR + I_{DISCH} x T/Ceff(T)

Where Ceff(T) = DC capacitance x % at time T read from Fig 8.

Shorter pulses need less capacitance to support them, so the supercapacitors can support short pulses despite their slow frequency response.

Balancing options

In many applications a voltage > 2.7V but ≤ 5.5V is required. For these applications 2 supercapacitor cells are connected in series in dual cell modules such as the CAP-XX GY2 series which is rated to 5.5V. These cells should have a balancing circuit to ensure that the cell voltages remain approximately equal or the cell with the lower C will have a higher voltage across it, causing it to age faster than its companion cell, hence losing even more C until it goes over voltage. This is a reason why a balancing circuit should aim to maintain the voltage across each cell equal, rather than just prevent over-voltage. As an example, if the dual cell module was at 5.0V and there was over-voltage protection circuits that prevented each cell from exceeding 2.7V, then module could have one cell at 2.7V and the other at 2.3V. The cell at 2.7V will age faster than the cell at 2.3V and will age faster than if both cells were held at 2.5V shortening module life.

In the GY2 series modules there is a PCB connecting the 2 cells. The voltage between the 2 cells must be balanced. This PCB can have one of two balancing options:

1. Option “R” as the last character in the GY2 series part number.
   A pair of balancing resistors are fitted, one resistor across each cell. The balancing resistors increase leakage current drawn by the module. Leakage current increases with capacitance, so modules made with larger cells need lower value balancing resistors that draw greater balancing current to ensure good voltage balancing between the cells. The dual cell module table

2. Option “A” as the last character in the GY2 series part number.
   An op amp maintains the midpoint voltage = ½ the supercapacitor module terminal voltage. This solution maintains the midpoint voltage very accurately, responds more quickly as the supercapacitor charges and discharges and only adds ~1µA to leakage current.

If the application uses a supercapacitor charging IC that has an integrated supercapacitor midpoint balancing circuit, or there is a balancing circuit on the PCB, then order 2 x GY1 cells and place them in series. This makes the midpoint available to your balancing circuit. The dimensions of 2 GY1 cells placed next to each other are the same as a shrink wrapped GY2 series cell, refer to Dimensions on page 4 of this datasheet. Refer to the Application Whitepaper on Supercapacitor Cell Balancing under the DESIGN AIDS section of the CAP-XX website, www.cap-xx.com for more information on cell balancing.

Storage

CAP-XX recommends storing supercapacitors in their original packaging in an air conditioned room, preferably at < 30°C and < 50% relative humidity. CAP-XX supercapacitors can be stored at any temperature not exceeding their maximum operating temperature but storage at continuous high temperature and humidity is not recommended and will cause premature ageing.

Do not store supercapacitors in the following environments:

- High temperature / high humidity
- Direct sunlight
- In direct contact with water, salt, oil or other chemicals
- In direct contact with corrosive materials, acids, alkalis or toxic gases
- Dusty environment
- In environments subjected to shock and vibration

Soldering

When soldering it is important to not over-heat the supercapacitor to not adversely affect its performance. CAP-XX recommends that only the leads come in contact with solder and not the supercapacitor body.

Hand Soldering
Heat transfers from the leads into to the supercapacitor body, so the soldering iron temperature should be < 350°C soldering time should be kept to the minimum possible and be less than 4 seconds.

Wave Soldering
The PCB should be pre-heated only from the bottom and for < 60 secs with temperature ≤ 100°C on the top side of the board for PCBs ≥ 0.8mm thick. The table below lists suggested solder temperatures.

Solder temperature °C	Suggested solder time (s)
220	7
240	7
250	5
260	3

Reflow Soldering
Infrared or conveyor oven soldering techniques can be used providing the supercapacitor body is not subject to temperatures > 65°C. Do not use a standard reflow oven.

Transportation

All the supercapacitor cells in this datasheet store < 0.3Wh energy. The energy in watt-hours is calculated as: ½ x Capacitance x V_{rated}^2/3600. The largest cell in this range is 100F, so stored energy = ½ x 100 x 2.7^2 /3600 = 0.101Wh. Under regulation UN3499 there is no restriction on shipping these supercapacitors. Their shipping description is “Electrical Capacitors” with harmonized shipping code 8532.29.0040.