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GY SERIES SUPERCAPACITORS

with radial leads

Datasheet Rev1.2, September 2019

1. Electrical Specifications

The GY series of supercapacitors are cylindrical cells offering excellent value. They are available as single cells, or dual cell modules with a choice of cell balancing options.

Single cells

Part numbering code

G	Y	N	vvv	dd	mmm	S	ccc	R
Model	**Cylind-rical**	**no of cells** 1	**Voltage** 2R7 = 2.7V	**Diameter** 6C = 6.3mm 08 = 8.0mm 10 = 10mm 1B = 12.5mm 16 = 16mm 18 = 18mm	**Length (mm)** 012 = 12mm 068 = 68mm 120 = 120mm	**Tolerance** M ± 20% S +50% /-20% V +30% /-10%	**µF** Two digits + number of zeros. 155 = 1500000µF = 1.5F	**Lead format** R = radial S = 2 solder pins W = 4 Cu tabs

Rated Voltage: 2.7V
Temperature Range: -40°C to +65°C
Parameters measured at 25°C

CAP-XX Part no.	Cap (F)	ESR Max @ 1KHz (mΩ)	ESR Max @ DC (mΩ)	Dia (mm)	Length (mm)	DCL max @ 72 Hrs (µA)	Mass (gm)	Power Density (W/kg)	Energy Density (Wh/kg)
Radial Lead									
GY12R76C012S105R	1	240	1500	6.3	12	6	0.60	972	1.69
GY12R708012S105R	1	180	860	8	12	6	0.85	1209	1.20
GY12R708016S205R	2	100	360	8	16	10	1.05	2274	1.90
GY12R708020S335R	3.3	95	280	8	20	11	1.25	2526	2.70
GY12R708025S505R	5	85	220	8	25	15	1.70	2339	2.98
GY12R710020S505R	5	70	170	10	20	15	2.1	2441	2.40
GY12R710020S705R	7	70	170	10	20	18	2.4	2144	2.95
GY12R710025S705R	7	60	150	10	25	20	2.5	2303	2.80
GY12R710025M106R	10	60	150	10	25	30	2.8	2083	3.62
GY12R710030M106R	10	50	75	10	30	30	3.1	3800	3.30
GY12R71B020M106R	10	50	75	12.5	20	30	3.4	3454	3.00
GY12R71B030M156R	15	40	60	12.5	30	50	4.3	3359	3.50
GY12R71B035M226R	22	34	55	12.5	35	60	5.3	2824	4.17
GY12R716025M256R	25	27	50	16	25	60	7.2	2419	3.50
GY12R716030M306R	30	20	40	16	30	70	8.2	2644	3.70
GY12R718040M506R	50	18	20	18	40	75	12.7	3456	4.00
GY12R718060M107R	100	15	18	18	60	260	20.7	2352	4.90

Dual Cell Modules

Part numbering code

G	Y	N	vvv	dd	mm	S	ccc	L	B
Model	**Cylind-rical**	**no of cells** 2	**Voltage** 5R5 = 5.5V	**Diameter** 6C = 6.3mm 08 = 8.0mm 10 = 10mm 1B = 12.5mm	**Length (mm)** 012 = 12mm 068 = 68mm	**Tolerance** M ± 20% S +30% /-10% V +25% / -5%	**µF** Two digits + number of zeros.	**Lead alignment & package format** R,S,T = shrink wrap/radial – see dwg P,Q,O = plastic/radial – see dwg	**Balancing** R = Resistor* A = Active*

*R pair of balancing resistors, 0402 resistors, 100KΩ unless otherwise stated in the order,
*A = CAP-XX active balancing circuit which draws < 1µA. For active balancing, lead alignment, L, must be “S” or “Q”.

Rated Voltage: 5.5V
Temperature Range: -40°C to +65°C
Parameters measured at 25°C

CAP-XX Part no.*	Cap (F)	ESR Max @ 1KHz (mΩ)	ESR Max @ DC (mΩ)	Cell Diameter (mm)	Length (mm)	DCL max @ 72 Hrs (µA)*	Mass (gm)	Power Density (W/kg)	Energy Density (Wh/kg)
Shrink Wrap									
GY25R50814S474RR	0.47	380	1720	8	14	2	1.95	1124	1.00
GY25R50818S105RR	1	250	730	8	18	6	2.30	2143	1.80
GY25R50822S155RR	1.5	200	520	8	22	10	2.6	2676	2.40
GY25R51022S255RR	2.5	180	340	10	22	20	4.2	2537	2.50
GY25R51027S355RR	3.5	160	300	10	27	23	5.4	2200	2.70
GY25R51B22S505RR	5	120	150	12.5	22	25	7.0	3474	3.00
GY25R51B32M755RR	7.5	100	120	12.5	32	65	9.5	3195	3.30
GY25R51628M126RR	12.5	70	100	16	28	90	15.4	2342	3.40
Plastic Package									
GY25R50916S474PR	0.47	360	1470	8	16	2	6.6	376	0.30
GY25R50920S105PR	1	200	730	8	20	6	6.0	822	0.70
GY25R50924S155PR	1.5	190	530	8	24	10	6.3	1078	1.00
GY25R51125S255PR	2.5	140	330	10	25	20	9.5	1161	1.10
GY25R51130S355PR	3.5	120	310	10	30	23	9.8	1202	1.5

*Part numbers shown for lead orientation R, P and for balancing resistors, R.

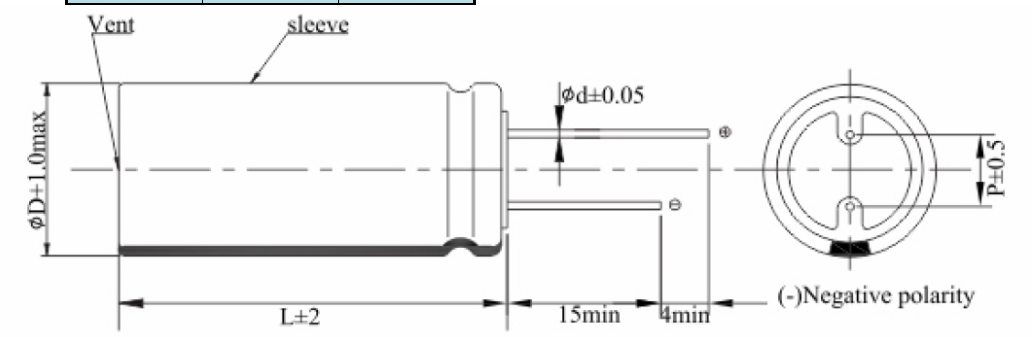
Applications:

- Energy Harvesting for wireless sensors
- Peak power support for GSM/GPRS transmission
- Last gasp power for remote meter status transmission
- Peak power support for locks & actuators
- Peak power support for portable drug delivery systems
- Short term bridging power for battery hot swap

2. Dimensions (mm)

GY1 Series Shrink Wrap Radial Lead 1F - 100F

D	P	d
6.3	2.3	0.6
8	3.5	0.6
10	5.5	0.6
12.5	5.5	0.6
16	8	0.8

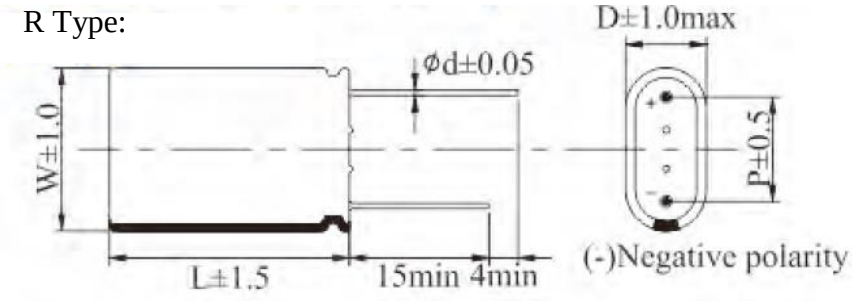


GY2 Series Shrink Wrap 0.47F – 12.5F, L = R, S or T.

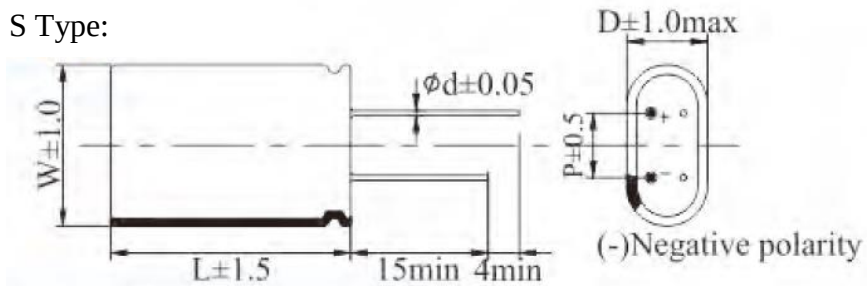
Note: All modules ordered with the active balance option must be S type.

Cell dia	D	W	P			Φd
			R	S	T	
8	8	16	11.5	8.0	4.5	0.6
10	10	20	15.5	10.0	5.0	0.6
12.5	12.5	25	18.0	13.0	7.5	0.6
16	16	32	24.0	16.0	8.5	0.6

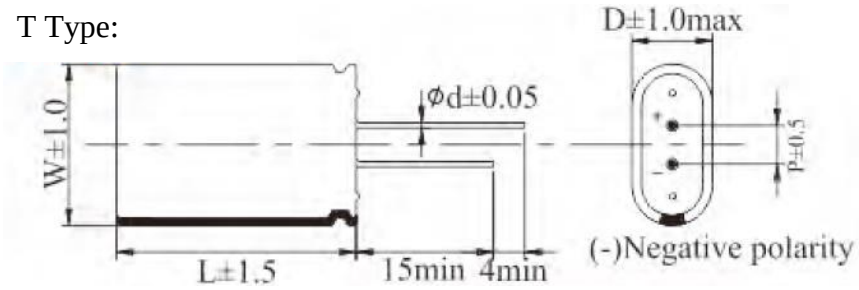
R Type:



S Type:



T Type:

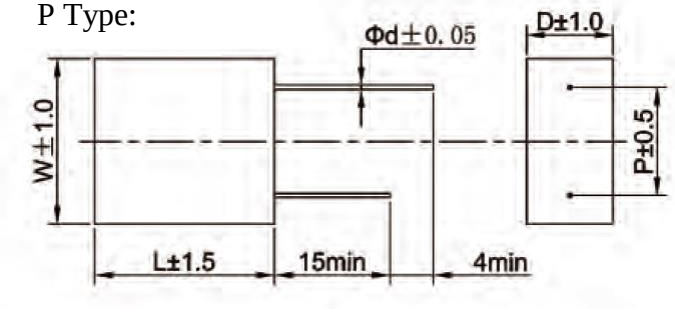


GY2 Plastic Package 0.47F – 12.5F, L = P, Q or O

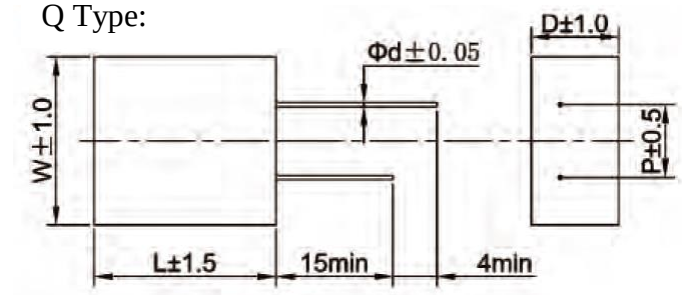
Note: All modules ordered with the active balance option must be Q type.

Cell dia	D	W	P			Φd
			P	Q	O	
8	9	18	11.5	8.0	4.5	0.6
10	11	23	15.5	10.0	5.0	0.6

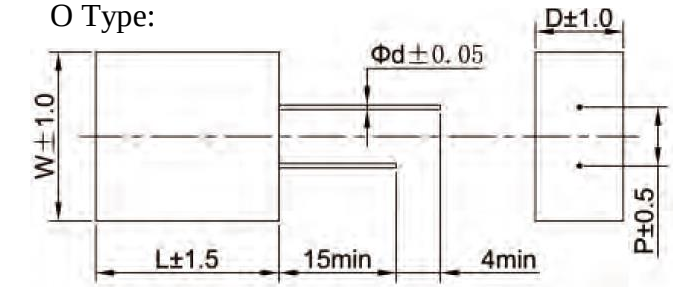
P Type:



Q Type:



O Type:



3. Measurement of capacitance

Capacitance is measured at 25°C using the method specified by IEC62391 shown in Fig 1. This measures DC capacitance. The capacitor is charged to rated voltage, V_R, at constant current, held at rated voltage for 30 minutes and then discharged at constant current. The time taken to discharge from 0.8 x VR to 0.4 x VR is measured to calculate capacitance as:

$I = 4 \times V_R \times C$ (mA)
$V_1 = 0.8 \times V_R$
$V_2 = 0.4 \times V_R$
$C = I \times (T_1 - T_2)/(V_1 - V_2)$

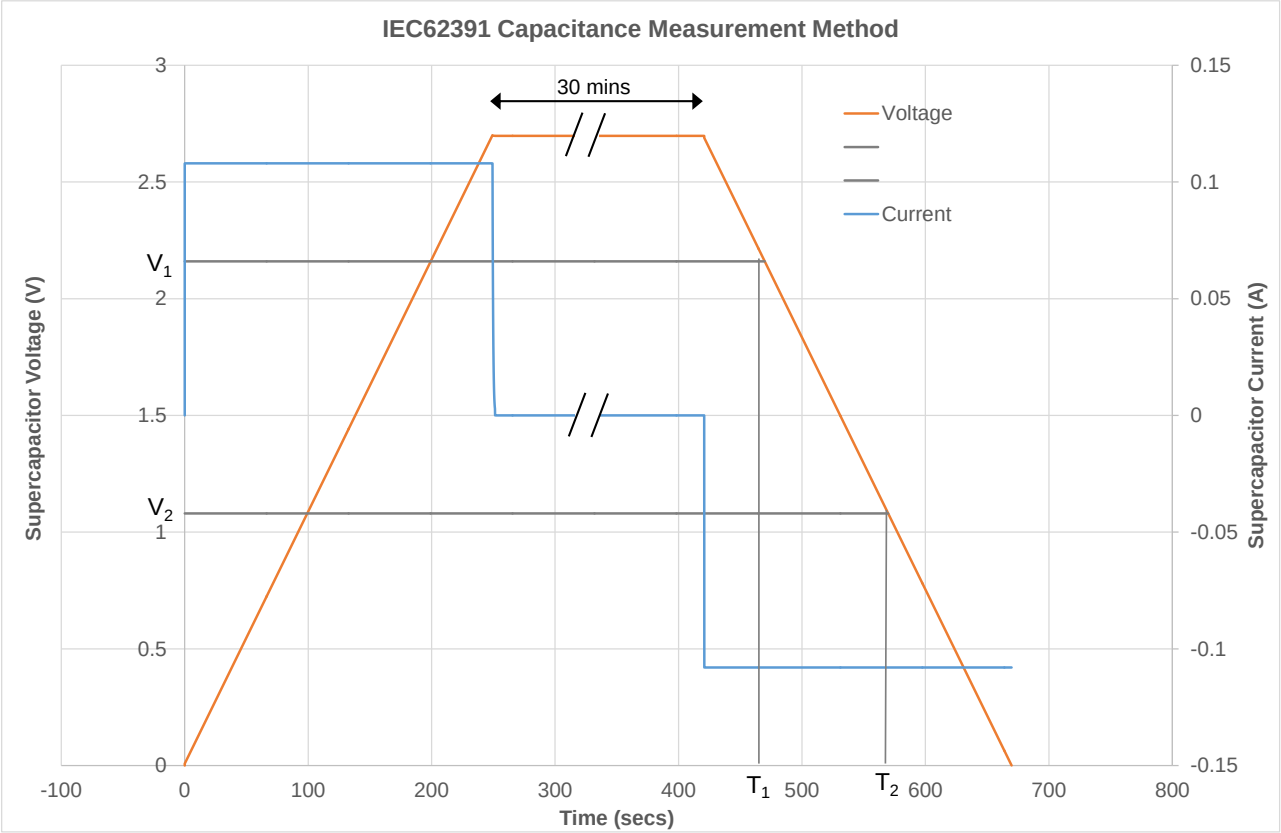


Fig 1: Capacitance measurement

4. Measurement of ESR

Equivalent Series Resistance (ESR) is measured at 25°C using the 6 step method shown in Fig 2. The measurement is carried out over 2 cycles measuring the difference in voltage from when discharge current is applied to when no current is applied. Referring to Fig 2:

$I_1 = I_2 = 75mA/F$

$ESR_{DC} = (ESR_{DC1} = ESR_{DC2})/2$

$ESR_{DC1} = (V_5 – V_4)/I_2$

$ESR_{DC2} = (V_{11} – V_{10})/I_2$

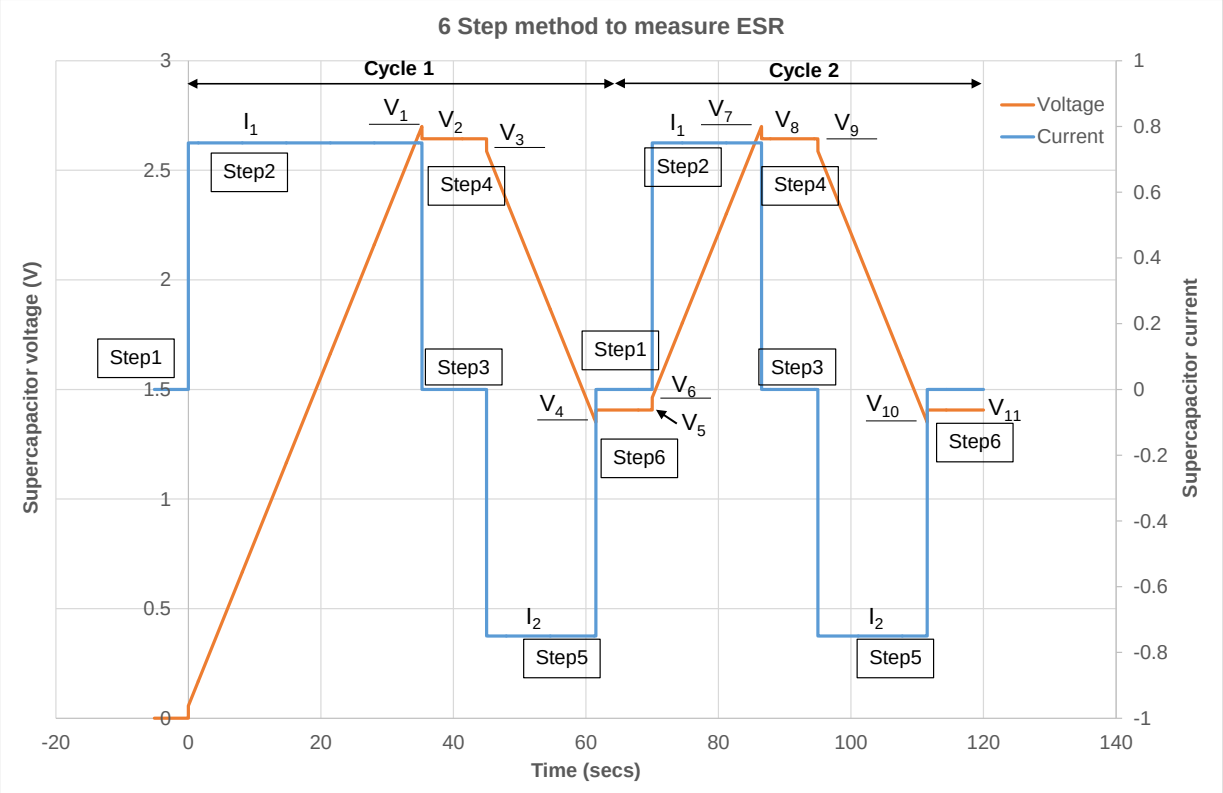


Fig 2: ESR Measurement

5. Measurement of Leakage Current

Leakage current is measured by holding the supercapacitor at rated voltage at 25°C and measuring the current drawn through a high value resistor, typically 1KΩ or 2.2KΩ. The leakage current decays over time as shown in Fig 3 which shows the leakage current for 4 samples each of 10F, 15F, 22F and 25F supercapacitors. Leakage current is typically 1µA/F but the datasheet quotes the maximum values. Leakage current in the datasheet is quoted after 72hrs at rated voltage.

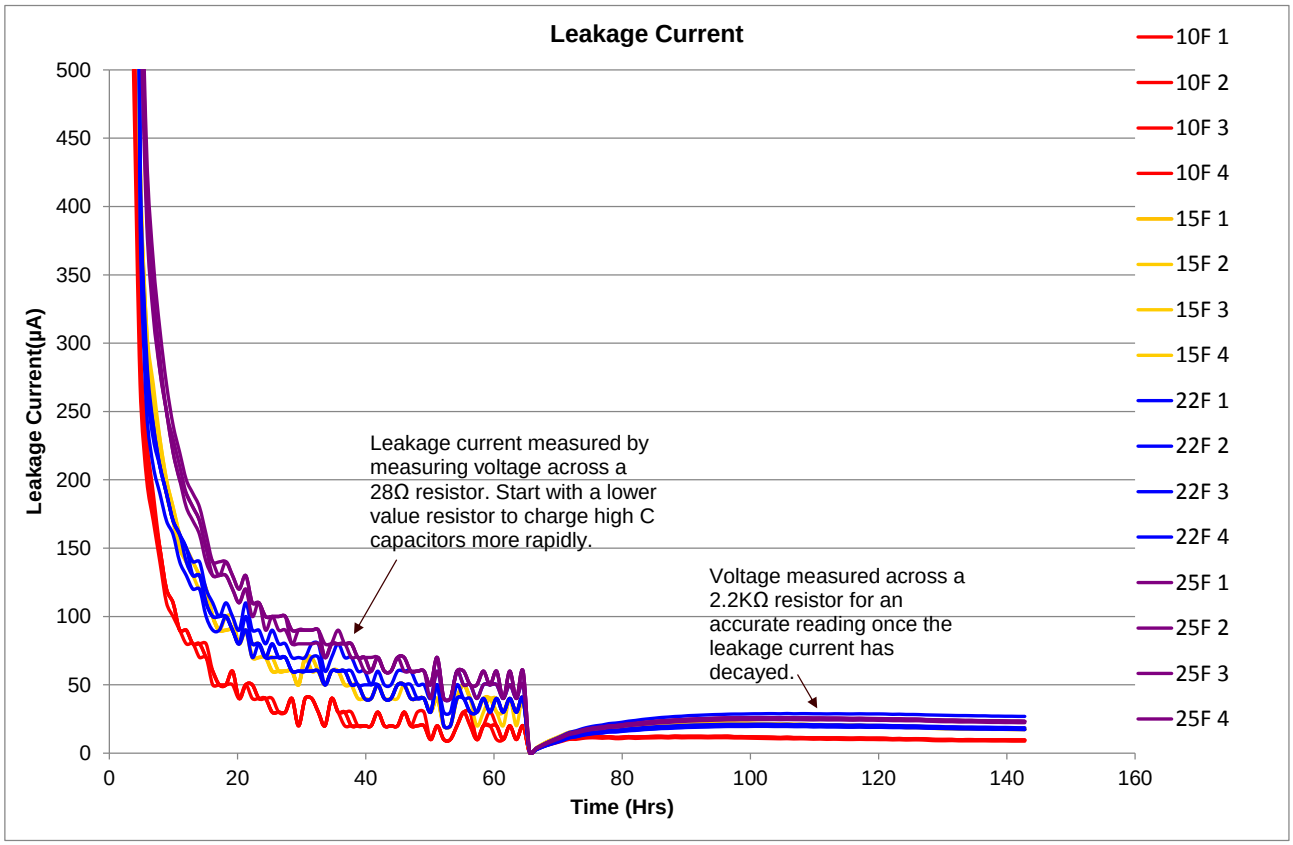


Fig 3: Leakage current measurement

6. Variation in DC Capacitance and ESR with temperature

Figure 4 shows that DC capacitance does not vary with significantly over the operating temperature range of -40°C to +65°C.

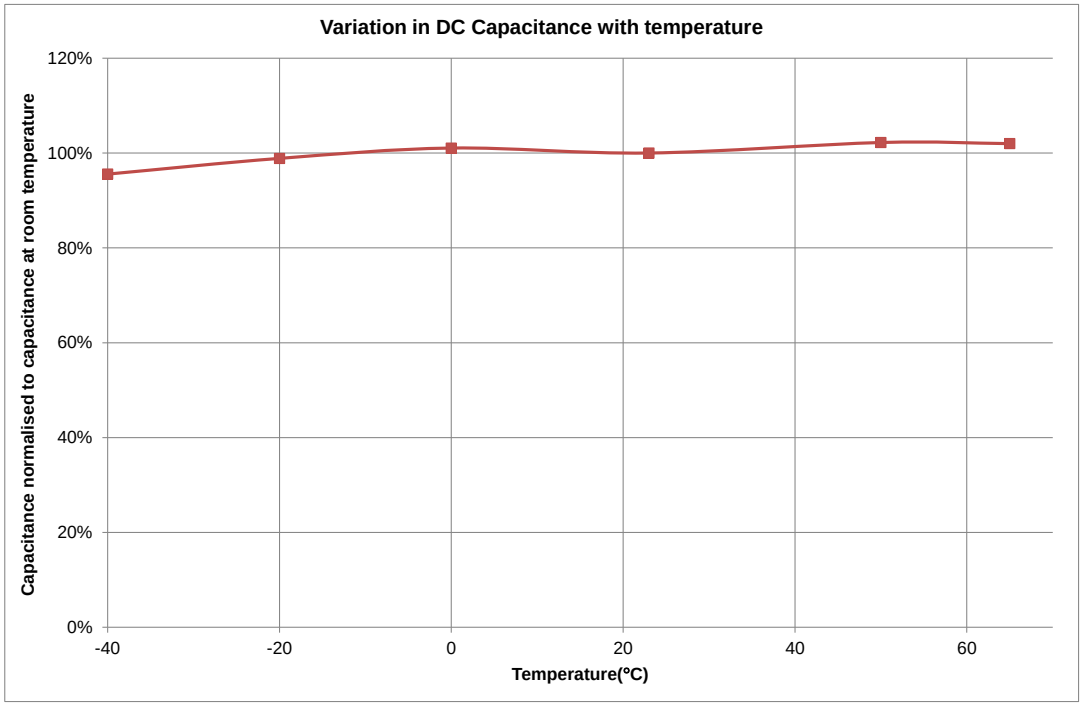


Fig 4: Variation in DC Capacitance over the operating temperature range

Figure 5 shows variation in DC ESR over the operating temperature range.

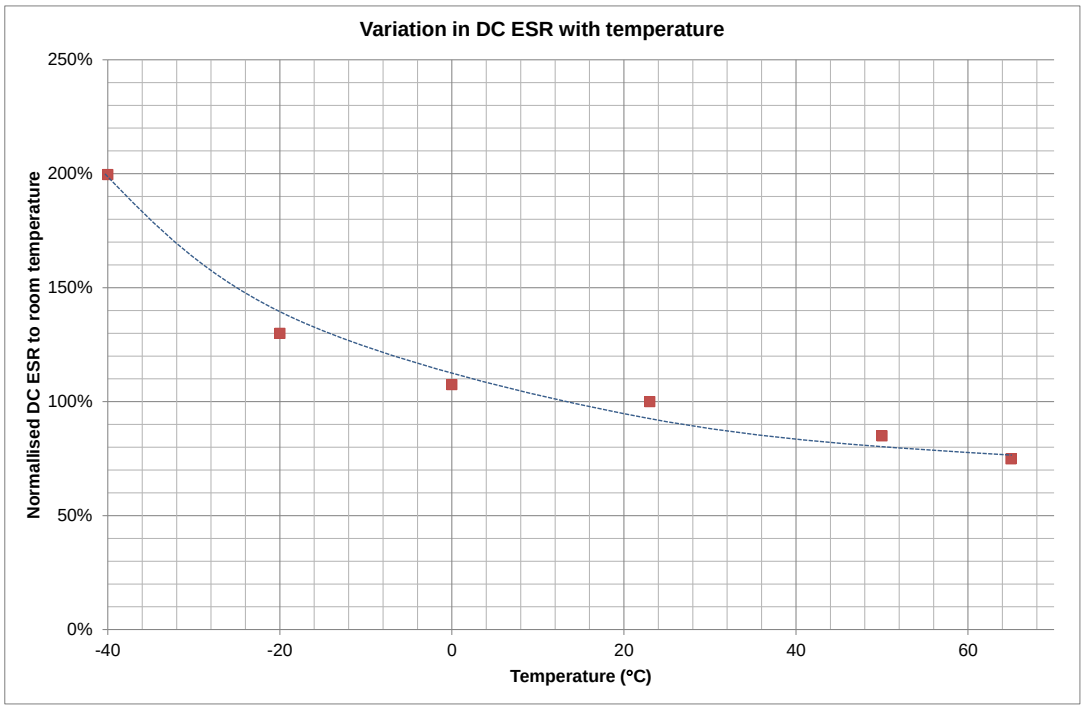


Fig 5: Variation in DC ESR over the operating temperature range

From Figure 5, ESR_{DC} at -40°C is double ESR_{DC} at room temperature. ESR_{DC} at 65°C is ~75% of ESR_{DC} at room temperature. The variation in ESR with temperature is due to the change in the mobility of ions in solution in the electrolyte.

7. Peak Current

Peak current is limited by Vrated/(ESR + R_L) where R_L is the load resistance including parasitic resistance such as PCB traces. The current then decays and is given by :

$$[Vrated/(ESR + R_L)].e^{-t/[(ESR+RL).C]}$$

where t = time in seconds. At high peak current, the supercapacitor discharges rapidly so that self heating due to the high current is negligible. Table 1 Shows short circuit current for a range of supercapacitors initially charged to 2.7V at the instant the short circuit is applied and after 100ms. It also shows the temperature increase recorded due to the short circuit.

Table 1:

Capacitance (F)	Instantaneous peak current (A)	Current after 100ms (A)	Temperature rise (°C)
25	58	44	2
15	40	26	2
10	40	26	3
5	20	15	1.5
3.3	20	13	2.8
2	15	10	1.5
1	15	7	1

In all cases the temperature rise is not significant. A one-time peak current pulse is only limited by the ESR_{DC} + Load resistance, not by any thermal limitations.
The voltage drop when a constant current pulse of duration τ is applied =

$$V_{INIT} - V_{FINAL} = I.ESR_{DC} + I.\tau/C$$

Where:

I = constant current
τ = duration of constant current
V_{INIT} = the initial voltage when the current pulse is first applied
V_{FINAL} = the supercap voltage at the end of the pulse

Re-arranging terms, the maximum current that can be sustained for a time τ, when the supercapacitor is initially charged to rated voltage, V_R, and discharged to V_{MIN}, the minimum voltage that supports the given application =

$$I_{MAX} = \frac{V_R - V_{MIN}}{ESR_{DC} + \frac{\tau}{C}}$$

For constant power where I increases as V decreases to keep V x I = constant, there is no closed form solution. Use the Fixed Power worksheet in the file BackpPower_VoltageDecay simulator on the CAP-XX website to determine the min voltage after applying a constant power for a given time.

8. Maximum Continuous Current

Continuous current flow into/out of the supercap will cause self heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, and then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 6 shows the increase in temperature as a function of RMS current for various supercapacitors.

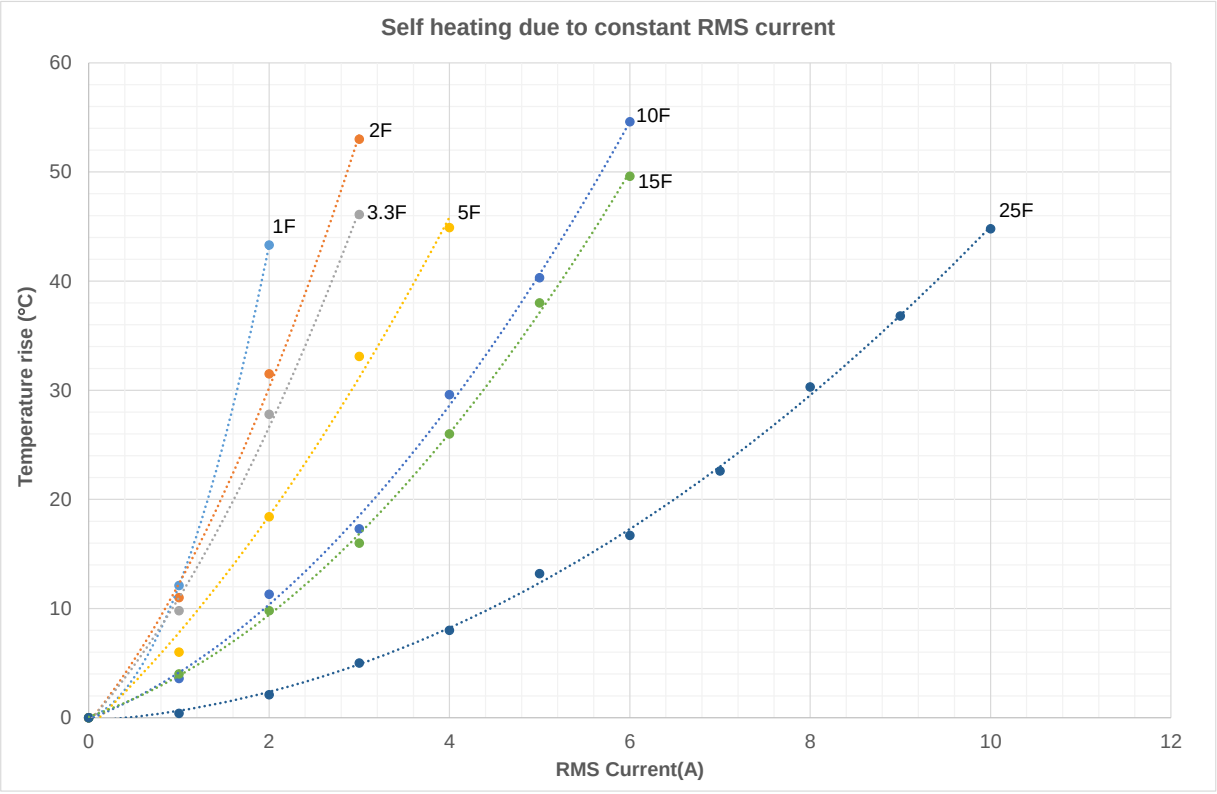


Fig 6: Self heating with RMS current for various supercapacitors

Supercapacitors with C > 25F will have a lesser temperature increase than the curve for the 25F supercapacitor in Fig 4. From Fig 4, the maximum RMS current in an application can be calculated. For example, if the ambient temperature is 40°C, and the maximum operating temperature for the supercapacitor is 65°C, then the maximum RMS current for a 10F supercapacitor should be limited to 3.6A, which causes a 25°C temperature increase.

9. Frequency Response and effective capacitance (Ceff)

Figure 7 show the frequency response for the 10F, GY12R710030S106R supercapacitor which is typical of the GY series.

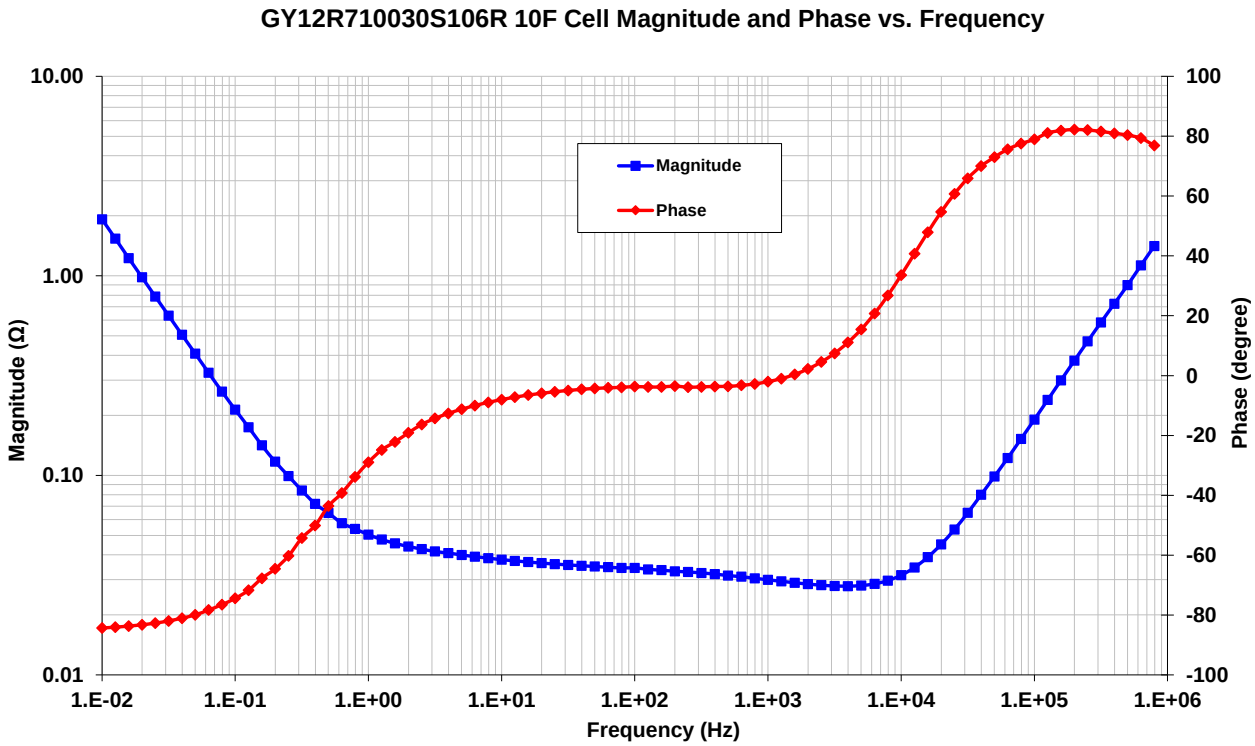


Fig 7: Magnitude and Phase Frequency Response for 10F cell, GY12R710030S106R

The magnitude curve shows capacitance starts to roll off at ~6Hz, while the phase curve crosses -45° at ~6Hz. This may lead to a false conclusion that the GY supercapacitor range cannot support short pulses. However, Fig 8 shows this 10F cell supporting a class 10 GPRS pulse train with 1.15ms pulses and a 4.6ms period. The supercapacitor has much lower ESR_{DC} than the charging source, so during the 1A pulse, the charging source is supplying 0.4A and the supercapacitor is supplying 0.6A. In between pulses the charging source is supplying 260mA. The I_discharge waveform has 1.15ms pulses which have significant components at 9.5KHz. That these pulses are square indicates that the supercapacitor has excellent pulse response despite the frequency response of Fig 7. This is explained by the concept of effective capacitance or Ceff. Consider the 1A, 100ms pulse of Figure 9. The voltage drop from 2.696V to 2.662V is the voltage drop due to ESR = Discharge_Current x ESR_{DC}. From this we can determine ESR_{DC} = (2.696V – 2.662V)/1.05A = 32mΩ. The voltage drop from 2.662V to 2.636V is due to capacitance discharge. Since Discharge_Current is constant, this should be a straight line, shown in Fig 9 as the slope = Discharge_Current/Ceff(100ms). The rounded leading edge of the voltage drop due to capacitance discharge is due to the frequency response of the supercapacitor. CAP-XX has created the concept of effective capacitance for a given pulsewidth, Ceff(pulsewidth) to translate this frequency response to the time domain and enable easy calculation of voltage drop for a given pulsewidth.

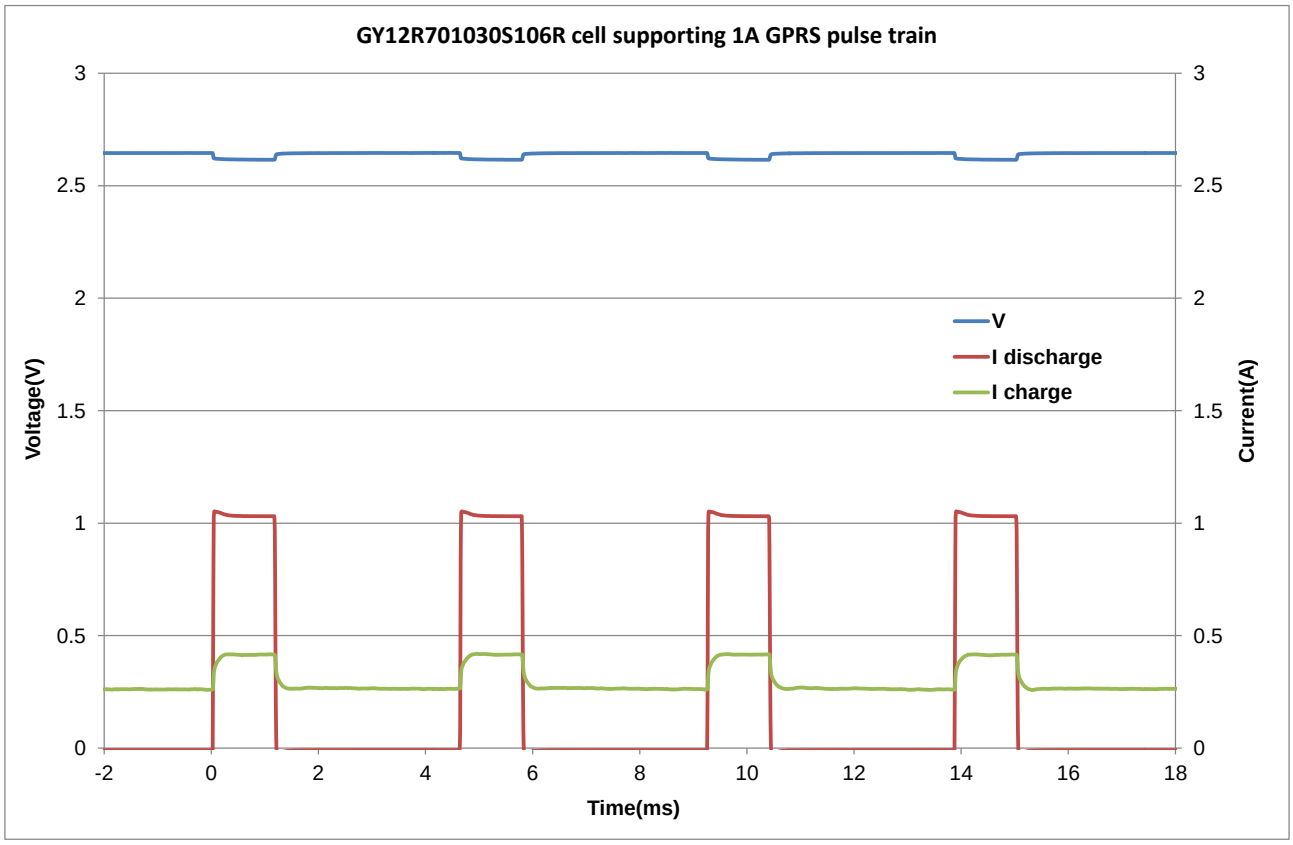


Fig 8: Pulse response of a GY12R701030S106R

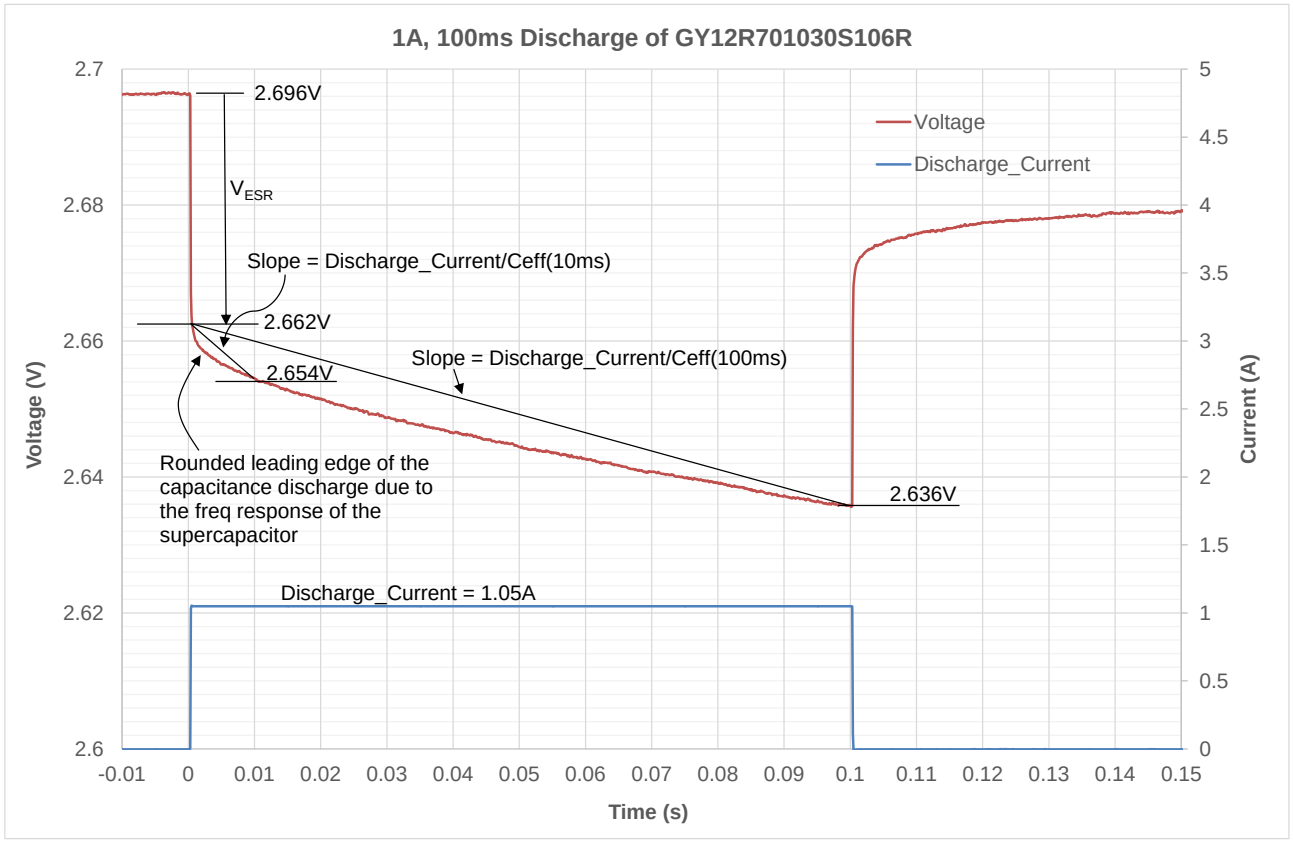


Fig 9: Discharge pulse illustrating the concept of Ceff

In Fig 9, consider the voltage drop due to capacitance after 10ms = 2.662V – 2.654V = 8mV. Therefore Ceff(10ms) = Discharge_Current x 10ms/Voltage drop(10ms) = 1.05A x 0.01s/0.008V = 1.3F. The voltage drop due to capacitance after 100ms = 2.662V – 2.636V = 26mV. Ceff(100ms) = 1.05A x 0.1s/0.026V = 4.0F. Fig 10 shows Ceff as a % of DC capacitance for the GY series of supercapacitors.

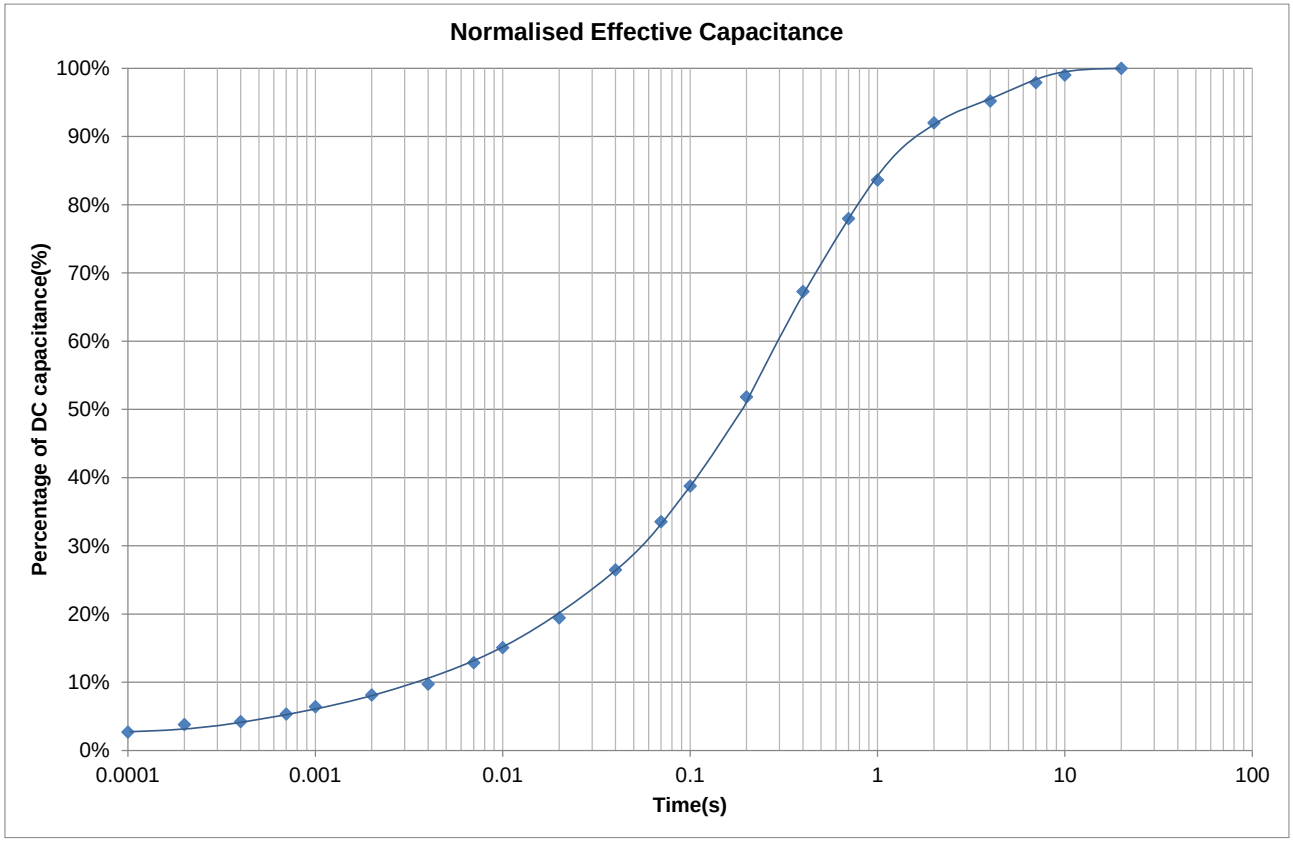


Fig 10: Normalised effective capacitance for GY series supercapacitors

From Fig 10, Ceff(1ms) = 6% x DC capacitance. In the case of Fig 8, with 1.15ms, 1.05A pulses supported by a GY12R710030S106R, Ceff = 6% x 10F = 0.6F. Therefore, the voltage drop during the pulse = 1.15ms x 1.05A / 0.6F = 2mV. This explains Fig 8 where the pulses appear square.

For any given pulsewidth, T, with a constant discharge current I_{DISCH}, the voltage drop is given by:

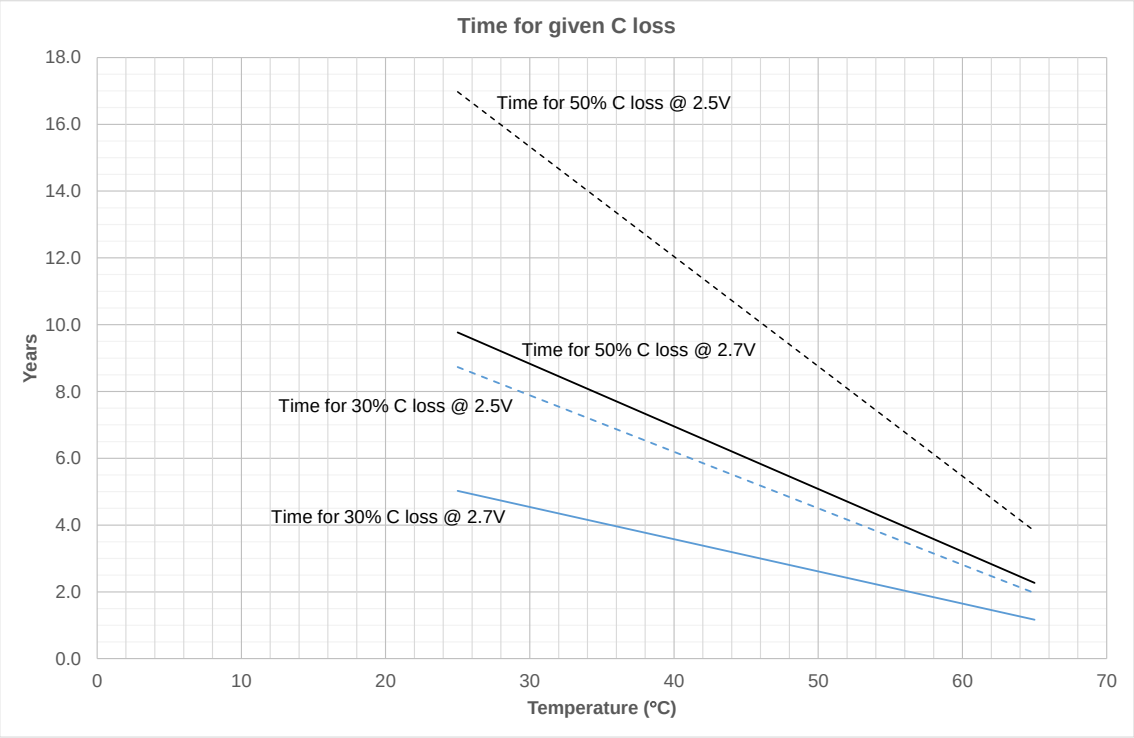
$V_{drop} = I_{DISCH} \times ESR_{DC} + I_{DISCH} \times T/Ceff(T)$

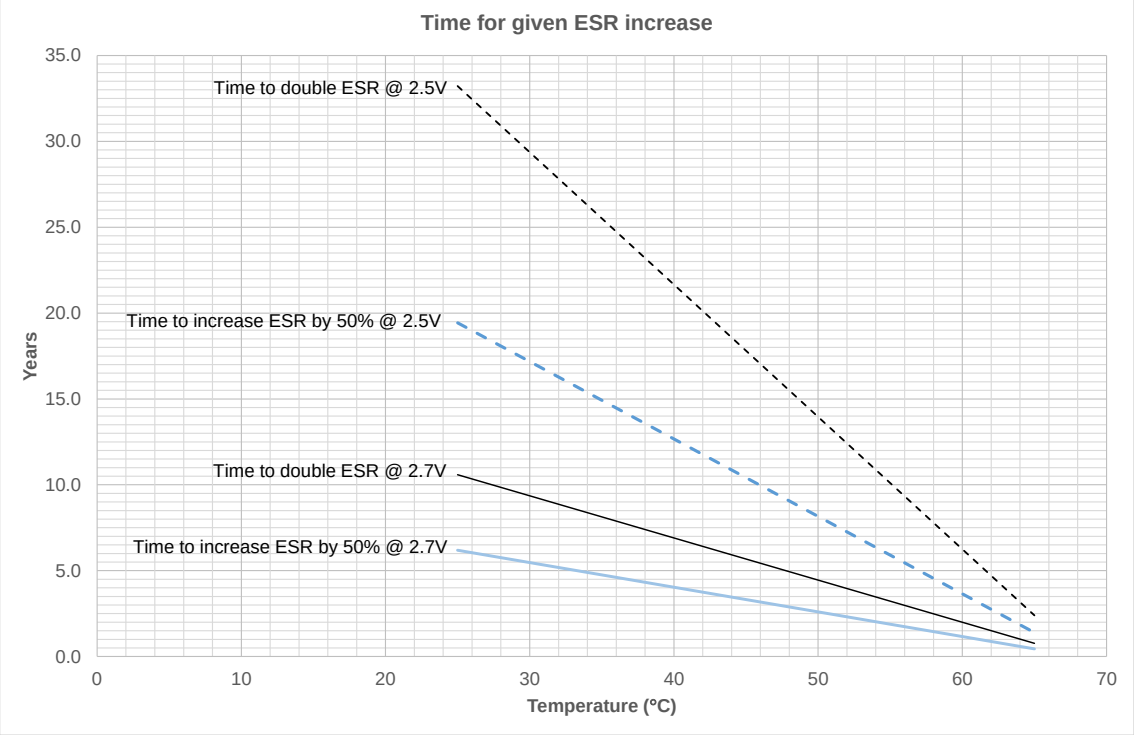
Where Ceff(T) = DC capacitance x % at time T read from Fig 10.

Shorter pulses need less capacitance to support them, so the supercapacitors can support short pulses despite their frequency response.

10. Operating Life

Supercapacitors slowly age over time with a loss of capacitance and increase in ESR. The rate of ageing depends on the operating voltage and temperature. The life will depend on the rate of C loss / ESR increase, the initial C and ESR of the supercapacitor, and the minimum C / maximum ESR that still supports your application. You can increase life in your application by simply starting with a higher C / lower ESR supercapacitor.





11. Balancing options

In many applications a voltage > 2.7V but ≤ 5.5V is required. For these applications 2 supercapacitor cells are connected in series in dual cell modules such as the CAP-XX GY2 series which is rated to 5.5V. These cells should have a balancing circuit to ensure that the cell voltages remain approximately equal or the cell with the lower C will have a higher voltage across it, causing it to age faster than its companion cell, hence losing even more C until it goes over voltage. This is a reason why a balancing circuit should aim to maintain the voltage across each cell equal, rather than just prevent over-voltage. As an example, if the dual cell module was at 5.0V and there was over-voltage protection circuits that prevented each cell from exceeding 2.7V, then module could have one cell at 2.7V and the other at 2.3V. The cell at 2.7V will age faster than the cell at 2.3V and will age faster than if both cells were held at 2.5V shortening module life.

In the GY2 series modules there is a PCB connecting the 2 cells. This PCB can have one of two balancing options:

1. Option “R” as the last character in the GY2 series part number.
   A pair of balancing resistors are fitted, one resistor across each cell. The balancing resistors increase leakage current drawn by the module. Unless otherwise specified, 680KΩ resistors are fitted, increasing leakage current by 4µA at 5.5V.

2. Option “A” as the last character in the GY2 series part number.
   An op amp maintains the midpoint voltage = ½ the supercapacitor module terminal voltage. This solution maintains the midpoint voltage very accurately, responds more quickly as the supercapacitor charges and discharges and only adds ~1µA to leakage current.

If the application uses a supercapacitor charging IC that has an integrated supercapacitor midpoint balancing circuit, or there is a balancing circuit on the PCB, then order 2 x GY1 cells and place them in series. This makes the midpoint available to your balancing circuit. The dimensions of 2 GY1 cells placed next to each other are the same as a shrink wrapped GY2 series cell, refer to section 13, Dimensions.

12. Vibration

Test parameters

Amplitude	1.5mm
Frequency	10 – 55Hz
Direction	X, Y, Z axis, 2hrs in each direction
Test Duration	6 hours

Acceptance criteria

Capacitance	≥ 70% of initial value
ESR	≤ 2 x initial value
Appearance	No remarkable defects

13. Storage

CAP-XX recommends storing supercapacitors in their original packaging in an air conditioned room, preferably at < 30°C and < 50% relative humidity. CAP-XX supercapacitors can be stored at any temperature not exceeding their maximum operating temperature but storage at continuous high temperature and humidity is not recommended and will cause premature ageing.

Do not store supercapacitors in the following environments:

- High temperature / high humidity
- Direct sunlight
- In direct contact with water, salt, oil or other chemicals
- In direct contact with corrosive materials, acids, alkalis or toxic gases
- Dusty environment
- In environments subjected to shock and vibration

14. Soldering

When soldering it is important to not over-heat the supercapacitor to not adversely affect its performance. CAP-XX recommends that only the leads come in contact with solder and not the supercapacitor body.

Hand Soldering:
Heat transfers from the leads into to the supercapacitor body, so the soldering iron temperature should be < 350°C soldering time should be kept to the minimum possible and be less than 4 seconds.

Wave Soldering:
The PCB should be pre-heated only from the bottom and for < 60 secs with temperature ≤ 100°C on the top side of the board for PCBs ≥ 0.8mm thick. The table below lists solder temperatures.

Solder temperature (°C)	Suggested solder time(s)	Maximum solder time (s)
220	7	9
240	7	9
250	5	7
260	3	4

Reflow Soldering:
Infrared or conveyor over reflow techniques can be used on these supercapacitors but do not reflow solder in a standard reflow oven.

15. Transportation

All the supercapacitor cells in this datasheet store < 0.3Wh energy. The energy in watt-hours is calculated as: ½ x Capacitance x V_{rated}^2/3600. The largest cell in this range is 100F, so stored energy = ½ x 100 x 2.7^2 /3600 = 0.101Wh. Under regulation UN3499 there is no restriction on shipping these supercapacitors. Their shipping description is “Electrical Capacitors” with harmonized shipping code 8532.29.0040.